Power Converters for Energy Storage Applications

Univ.-Prof. Dr. Petar J. Grbović

Innsbruck Power Electronics Lab. (*i-PEL*)

University of Innsbruck, Institute of Mechatronics
Innsbruck, Austria

The Presenter

Univ.-Prof. Dr. Petar J. Grbović

- Dipl. Ing. (B. Sc.) and the Magister (M.Sc.) The University of Belgrade, Serbia
- The Doctor (Ph.D), Laboratoire 'Électrotechnique et d'Électronique de Puissance de Lille, l'Ecole Centrale de Lille, France

>20 years R/D & Academic Experience

- RDA Co, Belgrade, Serbia
- CESET, Italy
- PDL Electronics, Ltd., Napier, New Zealand.
- Schneider Toshiba Inverter Europe, Pacy-Sur-Eure, France,
- General Electric Global Research, Munich, Germany.
- HUAWEI Technologies, Düsseldorf GmbH, Munich, Germany,
- Centre of Power Electronics and Drives, C-PED Lab., Roma TRE University, Italy.
- Innsbruck Power Electronics Laboratory (***i-PEL***), the University of Innsbruck, Austria.

Innsbruck Power Electronics Lab.

- **Innsbruck**, the Capital of Tirol, West of Austria

- **Leopold-Franzens University Innsbruck**, founded in 1669
- 27,769 students ; 11,359 (40.9%) International students
- 4 Nobel prize winners

- **Innsbruck Power Electronics Lab. (i-PEL)** recently founded by the University of Innsbruck and Infineon Technologies AG.
  - Applied Research in the field of Power Electronics
  - Cutting edge Power Semiconductors & Applications

Agenda

- PART ONE: Background of Power Conversion & Energy Storage
- PART TWO: Energy Storage (ES) Device
- PART THREE: Applications of ES
- PART FOUR: ES Selection & Design
- PART FIVE: Interface Power Converter

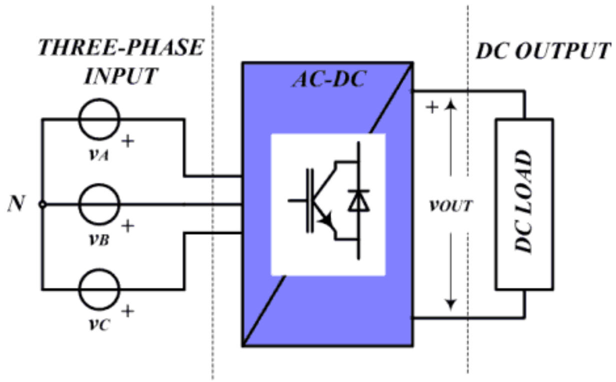
PART ONE
Background of Power Conversion & Energy Storage

1. Power Conversion
2. The need for Energy Storage
3. Energy Storage Technologies & Devices
4. Electrochemical Batteries
5. Flywheel Energy Storage
6. Ultra-capacitor Energy Storage
7. Ultra-capacitors versus Batteries

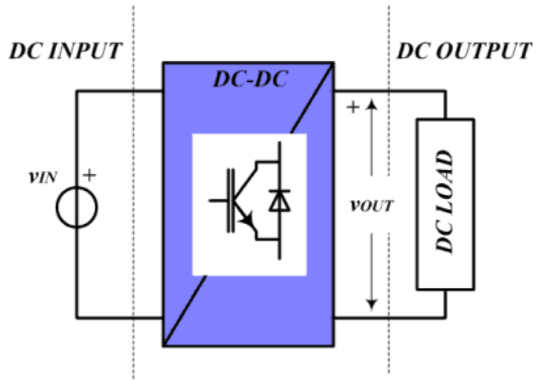
Power Conversion

- In general terminology, a power convertor is a device that converts energy from one form into another
  - **Electric to Electric**
  - Electric to Mechanic
  - Mechanic to Electric
  - Electric to Thermal
  - Thermal to Electric
- Static power convertor
  - Direct electric to electric energy conversion
  - Has no rotating elements, only semiconductor devices (diodes and transistors) and passives (inductors , transformers and capacitors)
  - Conversion of one electric quantity into another
    - Voltage, Current, Frequency, Phase

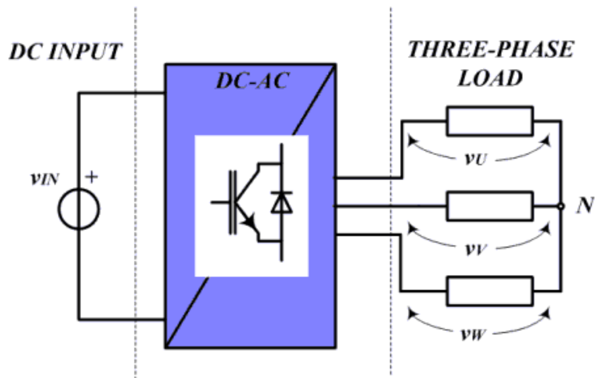
Power Conversion



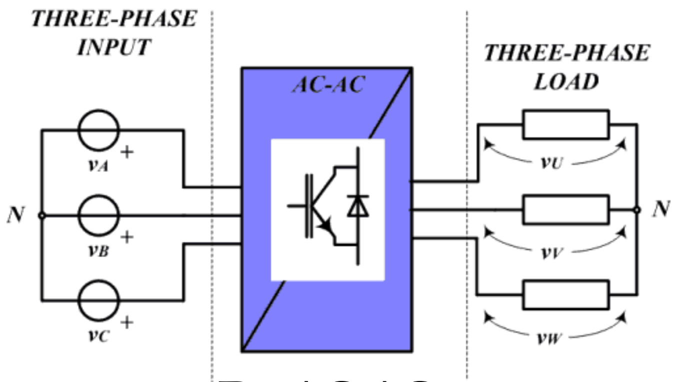
A. AC-DC



B. DC-DC



C. DC-AC



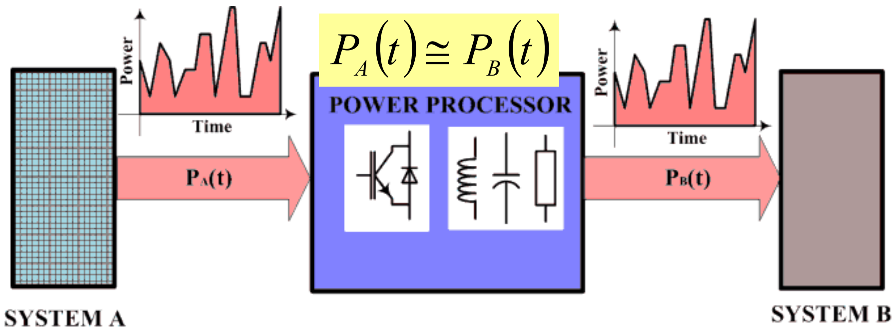
D. AC-AC

Possible combinations

E. A+B
F. B+B
G. B+C
H. A+C

The Need for Energy Storage

- Electric systems A & B are interconnected via a power processor
  1. A =the grid & B=electric drive
  2. A= wind mill & B=the grid
  3. A=the grid & B= a critical load (data center, hospital, etc., etc,.)
- The power processor: a static power converter, transformer, installation, etc., etc.
- The power processor has no energy storage capability
  - **Instantaneous power of both systems are equal.**

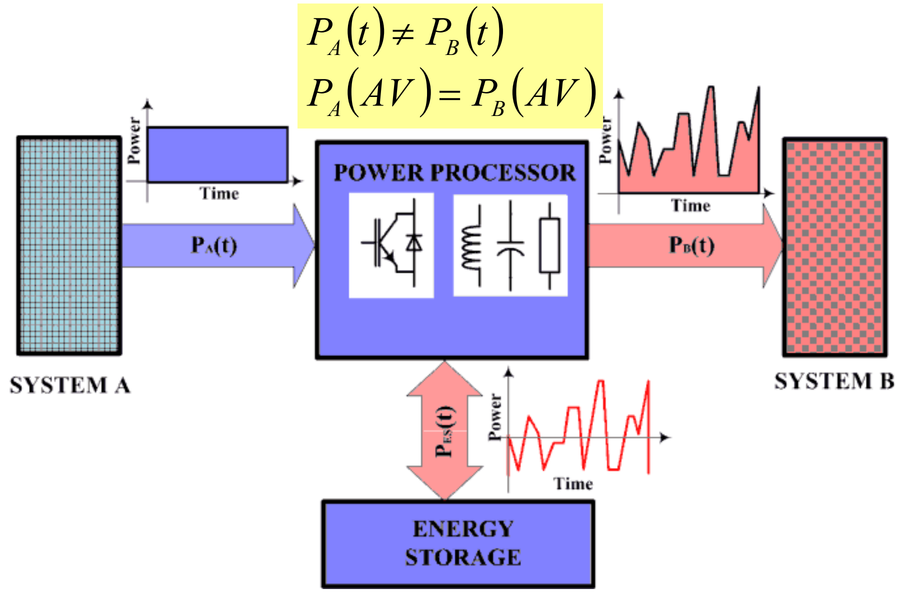


- The system is oversized
- Efficiency is reduced
- Peak power penalty
- Interruption cost and penalty

The Need for Energy Storage

1. A power processor with energy storage capability

- An energy storage device integrated within the power processor
- The energy storage device decouples the system A from the system B
- Instantaneous power
- Average power of the systems A & B remains the same



2. What is an energy storage device that can be used in power conversion applications?

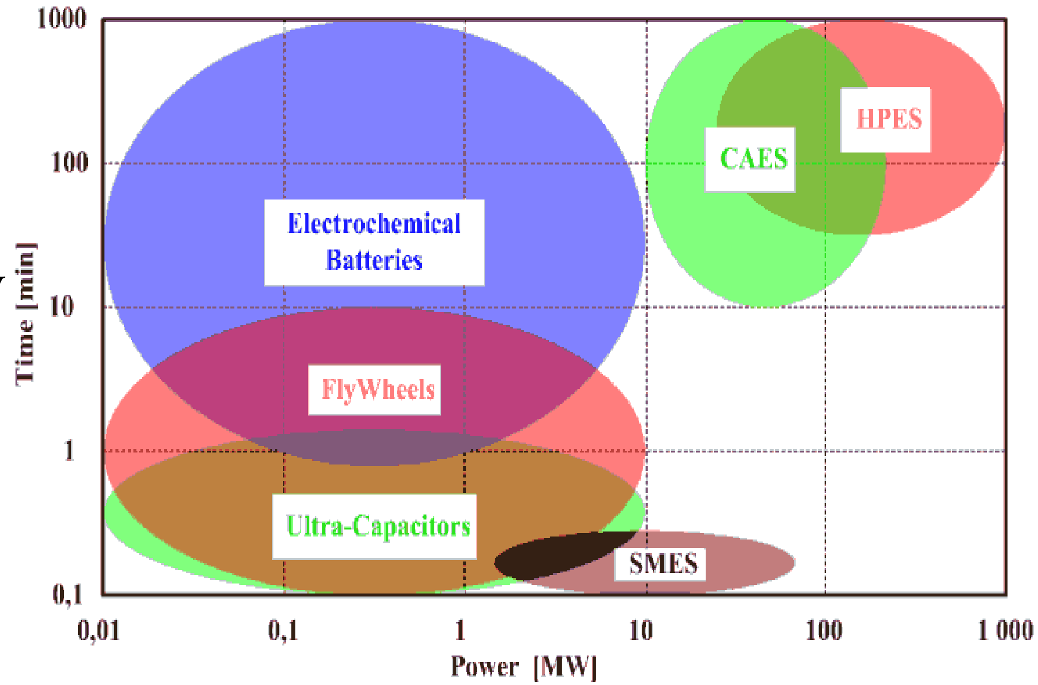
Energy Storage Devices

- Electric energy storage device is a device with ability to store electric energy and keep it stored for undefined period of time
  1. Direct Energy Storage (Simple electric devices), or
  2. (Indirect Energy Storage) Complex electro-mechanical or electro-chemical devices

<table>
<tr><th colspan="2">Direct Energy Storage</th><th colspan="5">Indirect Energy Storage</th></tr>
<tr><td>Magnetic Field</td><td>Electric Field</td><td colspan="3">Mechanical</td><td colspan="2" rowspan="2">Chemical</td></tr>
<tr><td>Inductors</td><td>Capacitors</td><td>Kinetic</td><td colspan="2">Potential</td></tr>
<tr><td>SMES</td><td>Ultra-capacitors</td><td>Flywheels</td><td>Hydro Pumped</td><td>Compressed air</td><td>Batteries</td><td>Fuel Cells</td></tr>
</table>

Energy Storage Devices

- CAES & HPES
  - Large scale utility applications
- SMES
  - High power short term utility applications
- Electrochemical Batteries
  - Long term, low & midium power applications
- Flaywheels & Ultra-capacitors
  - Short term, low & midium power applications



Electrochemical Batteries

- Secondary electrochemical batteries
  1. Convert electric energy into chemical energy (charging),
  2. Store chemical energy, and
  3. Convert chemical energy into electric energy (discharging)
- The most popular energy storage devices
- Composed of:
  1. Two electrodes of different material, and
  2. Electrolyte
- Electro-chemical action is a slow process
  - Charge and discharge rate are limited
    - Charge/Discharge power is limited
  - Life time and deep discharge cycling capability are limited

Electrochemical Batteries

State of the art electro-chemical batteries

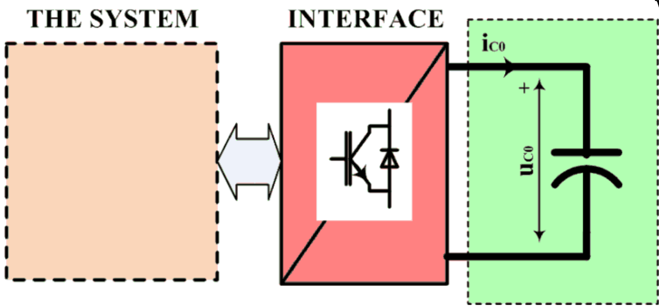
	Energy Density [Wh/kg]	Power Density [W/kg]	Life Time [Cycles]
Lead-Acid	20-35	25	100-2000
Lithium -Ion	100-200	360	500-2000
Lithium Polymer	200	250-1000	>1200
Nickel Cadmium	40-60	140-180	500-2000
Nickel-Metal Hydride	60-80	220	<3000
Sodium-Sulfur	120	120	2000
SiCB	50-100	800-3200	15,000-40,000

Ultra-capacitor Energy Storage

- An ultra-capacitor is a special kind of electrostatic capacitor
- **It is not an electrochemical battery!**
- Energy is stored directly as electric field between two charged plates

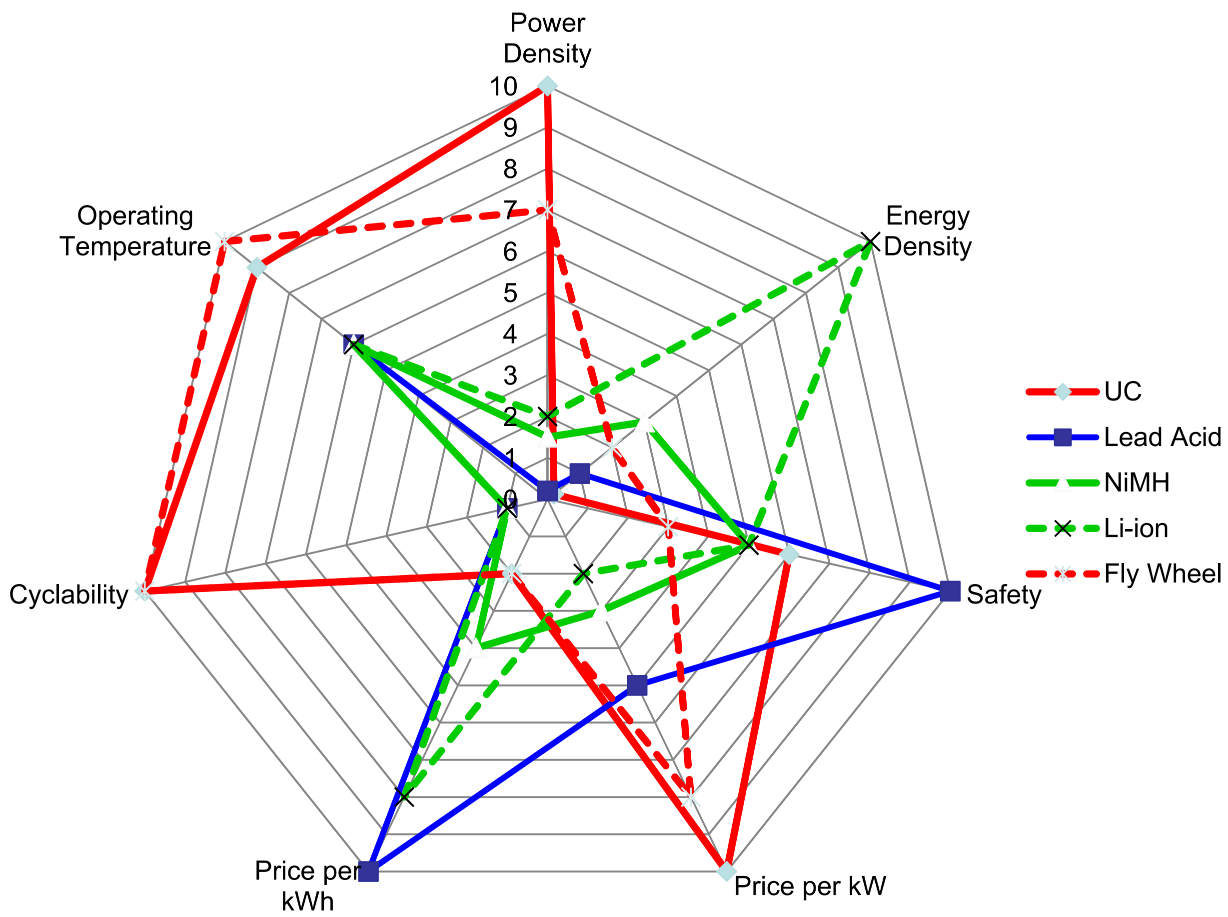
$$E = \frac{1}{2} C_0 u_{C0}^2$$

1. Capacitance of hundreds up to thousands of [F]
2. The cell voltage ~2.5 [V]
3. High energy density, 1 to 10 [Wh/kg] (>>> electrolytic capacitors)
4. High power density 5 to 20 [kW/kg]
5. Fast charge/discharge
6. High cycling capability <500 000 [cycles]
7. Wide range of operating temperature, from – 40 [°C] up to +60 [°C]



www.ultracapacitor.co.kr.

Comparison



Power Density
10
9
8
7
6
5
4
3
2
1
0
Energy Density
Safety
Price per kW
Price per kWh
Cyclability
Operating Temperature
UC
Lead Acid
NiMH
Li-ion
Fly Wheel

Ultra-capacitors versus Batteries

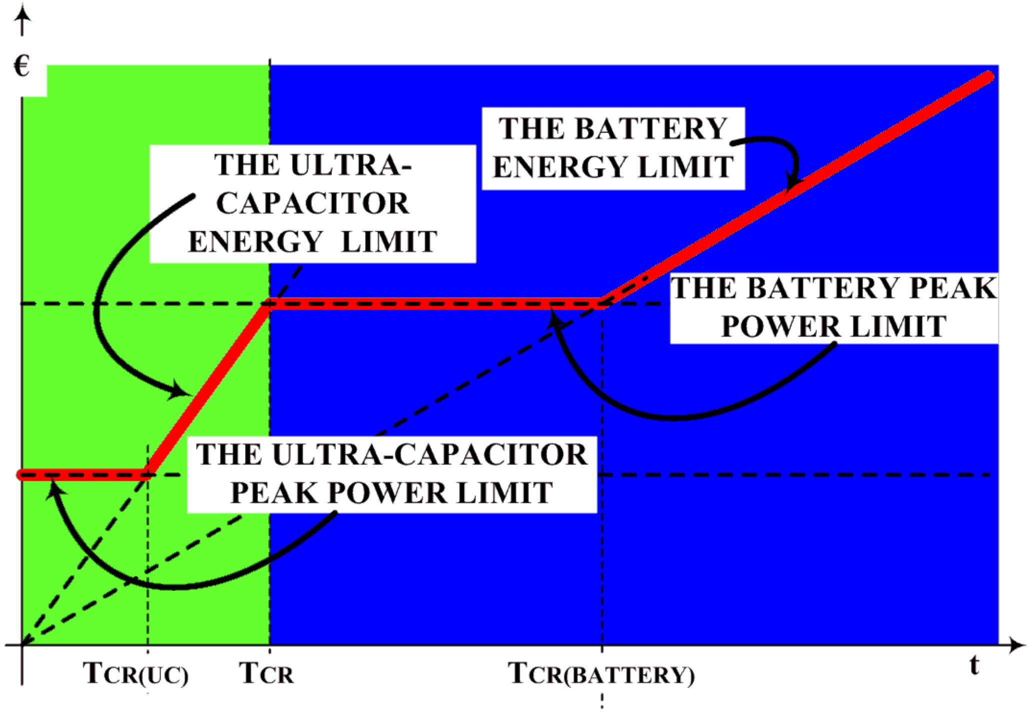
- Size and cost of an energy storage
  1. Energy Storage Capability
  2. Power Capability & Conversion Efficiency
  3. Cycling capability & Life time

If the charge/discharge time is shorter than T_{CR}

A. An ultra-capacitor is the solution,

B. Otherwise an electro-chemical battery is the solution

- Currently **T_{CR} =10 to 30s**



PART TWO
Ultra-capacitor Energy Storage Device

1. A bit of history of ultra-capacitors
2. How does ultra-capacitor work
3. Material
4. Technologies overview
5. Advantages and disadvantages
6. Ultra-capacitor macro model
7. Charge and discharge Methods
8. Frequency dependent losses and thermal aspects
9. Integration of the ultra-capacitor into power conversion system
10. Ultra-capacitors today and tomorrow

Ultra-capacitor History

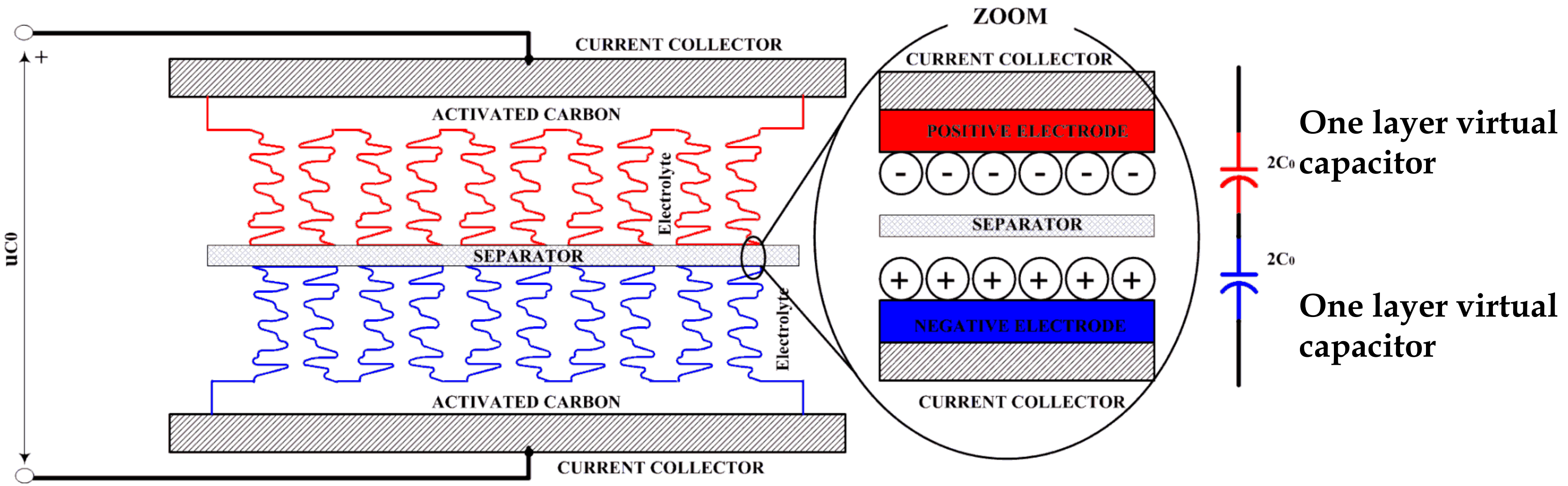
- The double layer capacitor effect was described by Helmholtz in 1879
- Almost a century after that, a first ultra-capacitor was patented by Standard Oil Company in 1966
- A decade after NEC developed and commercialized this device in 1978
- The first high power ultra-capacitor was developed for military applications by the Pinnacle Research Institute in 1982
- Ten years after, in 1992, the Maxwell Laboratory had started development of DoE ultra-capacitors for hybrid electric vehicles
- Today, the ultra-capacitors are commercially available from numerous manufacturers

How does ultra-capacitor work?

Ultra-capacitor is an electrochemical capacitor composed of:

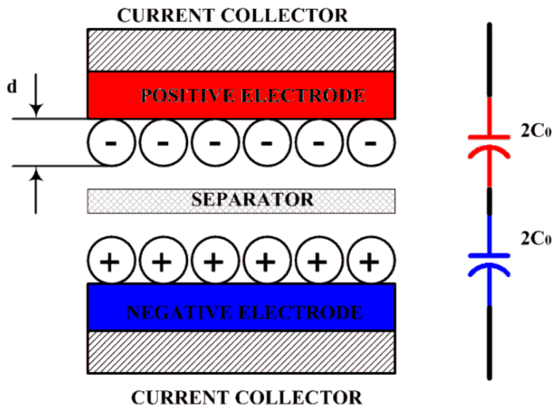
1. Two current collectors
2. Two electrodes made of porous conducting material (activated carbon…)
3. A separator, and
4. Electrolyte

- The electrodes are separated by the separator and immersed in the electrolyte



How does ultra-capacitor work?

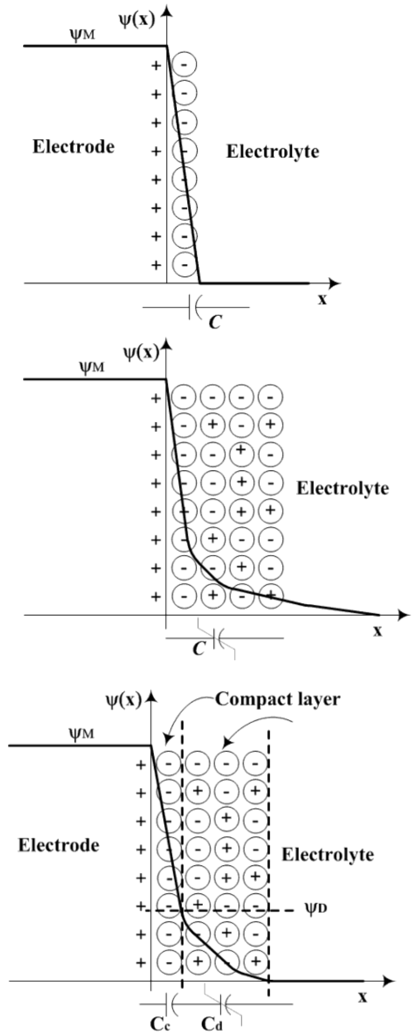
- Electrode is conducting and very porous material
- Positive and negative ions form a layer attached to the electrode surface
- Each layer forms a capacitor
  - The dielectric is a layer of ions. Relative permeability **ε_R~10**
  - The dielectric thickness is ***d***, diameter of the ions, approximately **d~10 Å**
  - Operating voltage is 1-3V, being limited by decomposition voltage of the electrolyte
  - The surface ***A*** is contact surface of the porous electrode, theoretically **A~2000m²/g** for activated carbon electrode



$$2C_0 = \varepsilon\varepsilon_R \frac{A}{d}$$

  - Theoretically, specific capacitance C~125F/g @ 2.5V ✡390kJ/kg
  - Overestimated capacitance, in reality it is 6 to 12F/g (5-10%)

How does ultra-capacitor work?



1. Simple double layer model is not accurate

$$C = \varepsilon \varepsilon_R \frac{A}{d}$$

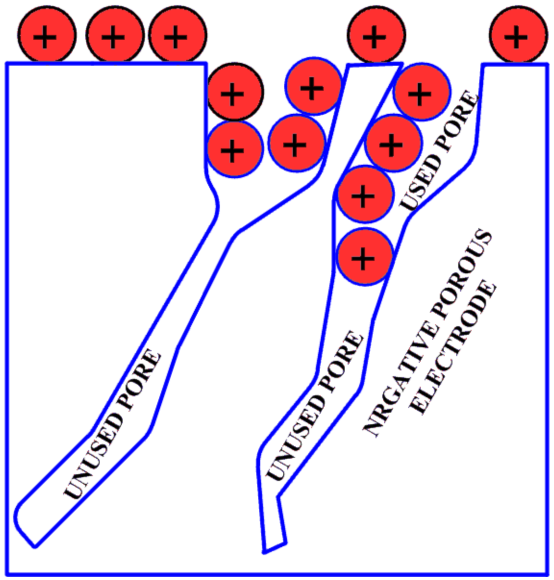
- Very first work, Helmholtz in 1853
  - A layer of electrolyte molecules attached to the electrode
  - Overestimated capacitance, no voltage dependency
- Gouy and Chapman, 1910 and few years later
  - Considered a space distribution of the charge

$$C' = Az\sqrt{\frac{2q^2 n_0 \varepsilon}{kT}}\, ch\left(\frac{z\Psi_M q}{2kT}\right)$$

- Stern, 1924
  - Real dimension of solvent molecules
  - The space charge in two layers compact layer and diffused layer

$$C'_D = Az\sqrt{\frac{2q^2 n_0 \varepsilon}{kT}}\, ch\left(\frac{z\Psi_D q}{2kT}\right)$$

How does ultra-capacitor work?



Zoomed in pore of porous activated carbon electrode. The ions penetrate only in large pores

2. The porous electrode contact surface is overestimated

- Theoretically A~2000m^2/g for activated carbon electrode
- Practically, 10 to 20 % of the theoretical one
- The electrode pores are not uniform
  - Large pores
  - Medium, and
  - Small pores
- Ions do not penetrate in medium and small pores.
- **The effective surface is much smaller than the theoretical one**

Ultra-capacitor Material

- Current collector
  a) Metal foil (Al, etc., etc.)
- Electrode
  a) Carbon (Activated carbon, Carbon nanotubes, Fibers)
  b) Metal oxides
  c) Polymers
- Electrolyte
  a) Organic (Operating voltage ~2.8V, Good energy density, High series resistance, Low power density, External balancing circuit is required)
  b) Aqueous (Operating voltage ~1V, Low series resistance, Good power density, Good voltage balancing even without external circuit)
- Separator
  a) Organic (Polymer, Paper)

Advanatges & Disadvanatges

Advantages

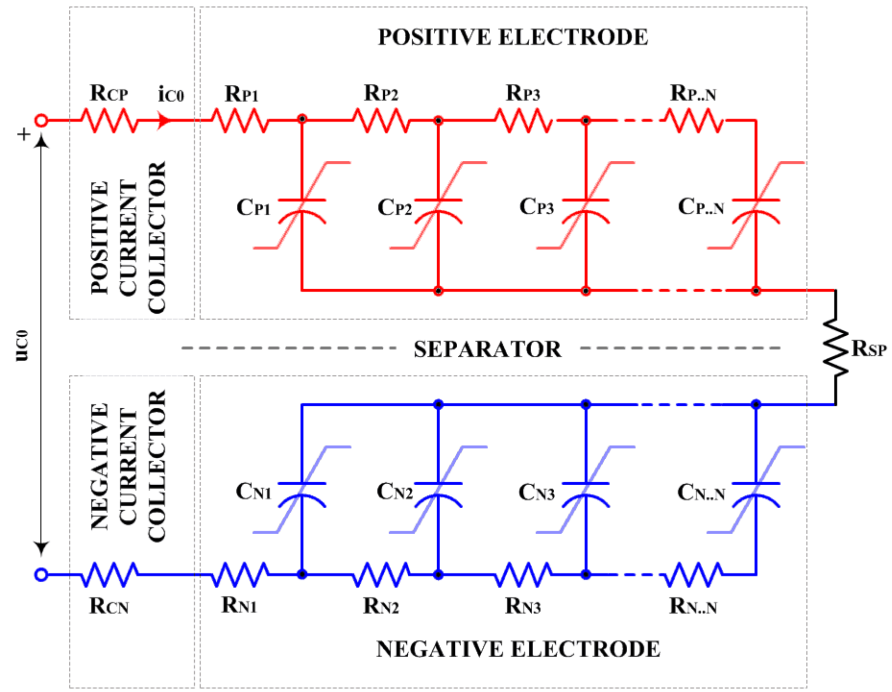
1. High specific power >10 [kW/kg]
2. Low internal resistance
3. High output power
4. High cycling capability >500 000 [cycles]
5. No chemical action
6. Long life ~20 years
7. Low cost per cycle
8. Very high rate of charge/discharge
9. Improved safety
10. Simple charge/discharge method

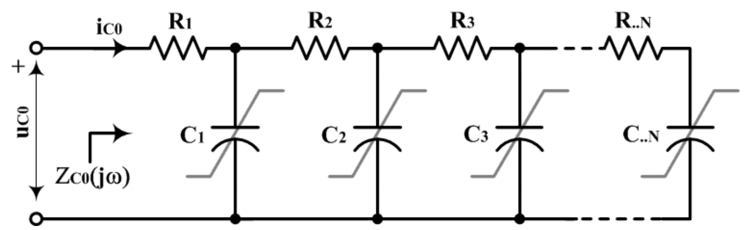
Disadvantages

1. Low specific energy <10 [Wh/kg] for standard ultra-capacitors
2. Voltage varies with state of charge Need for interface converter
3. High self-discharge rate
4. Low cell voltage. Need for series connection of cells into a module
5. Low internal resistance may create an issue in case of short circuit

Ultra-capacitor Macro Model

- Macro (Electrical) model
  - The control system analysis and synthesis, and
  - Losses calculation and thermal design
- Two main effects
  1. Voltage dependent capacitance $C = f(u_{C0})$
  2. The charge time/space distribution due to porosity of the electrodes
- Nonlinear transmission line
  - Nth order ***RLCG*** ladder network as an approximation
  - The inductance ***L*** and shunt conductance ***G*** (leakage) neglected



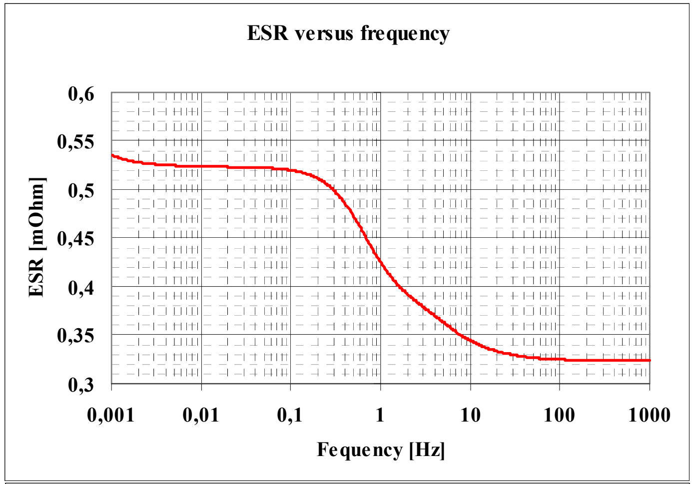


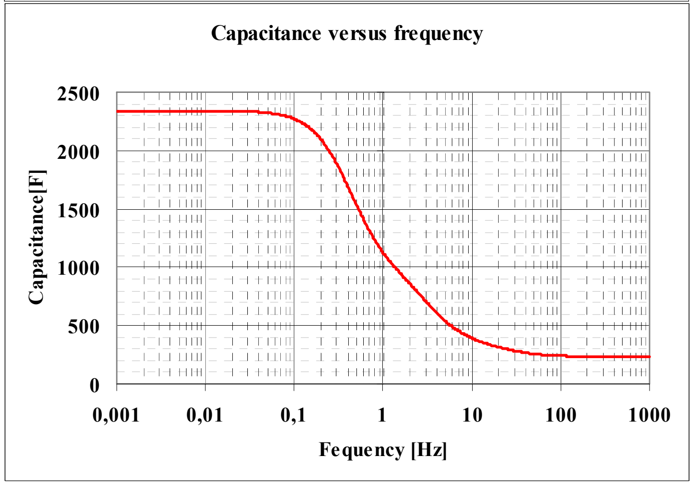
Ultra-capacitor Macro Model

- Nonlinear distributed network
- Voltage dependent capacitance and resistance
- Linearization around an operating point $u_{C0}=U_{C0}$
  - Small signal N_{th} order ladder RC network

$$Z_{C0}(j\omega)\Big|_{u_C=U_{C0}} = R_{C0}(\omega)\Big|_{u_C=U_{C0}} + \frac{1}{j\omega C_C(\omega)\Big|_{u_C=U_{C0}}}$$

  - ESR $R_{C0}(\omega)$ and capacitance $C_{C0}(\omega)$
  - Parasitic inductance is neglected at the frequency of interest

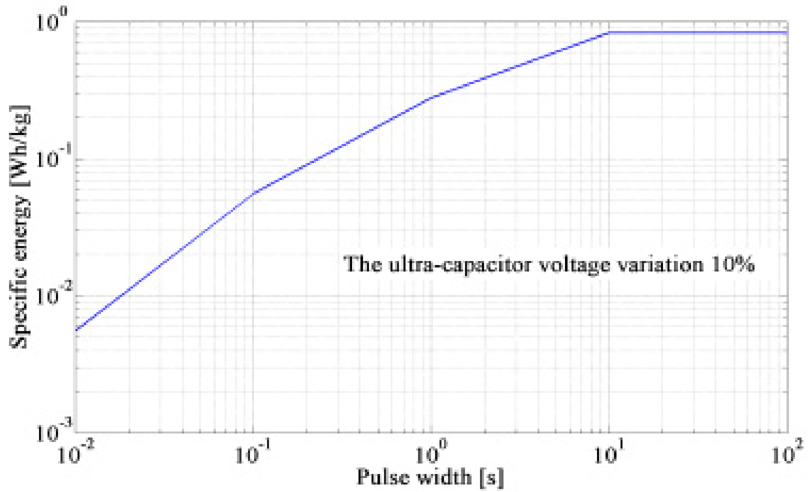




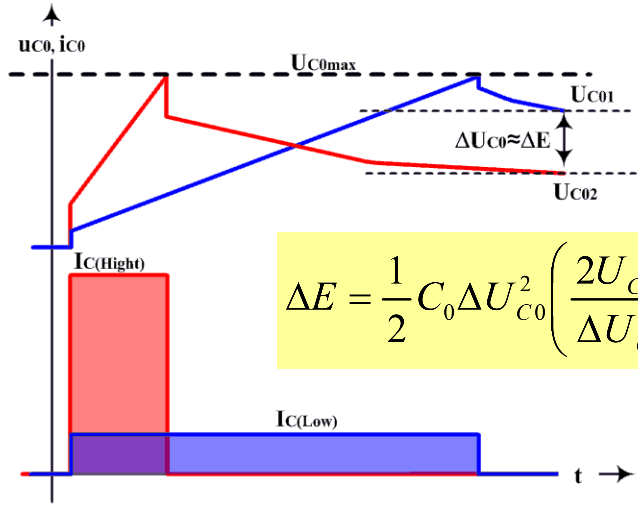
An example: 2500F ultra-capacitor cell. The parameters at $U_0=1V$

Frequency Dependent Capacitance

- The capacitance depends on frequency $C_{C0}(\omega)$
- Is it reflected to a real application and how?
- Specific energy depends on frequency (pulse width), Fig A
- The capacitor is charged with a short pulse and a long pulse, Fig B
  - Final state of charge is expected to be the same in both cases , but it is not



A. Specific energy versus pulse width



$$\Delta E = \frac{1}{2} C_0 \Delta U_{C0}^2 \left(\frac{2U_{C01}}{\Delta U_{C0}} - 1 \right)$$

B. Pulse width effect on final state of charge

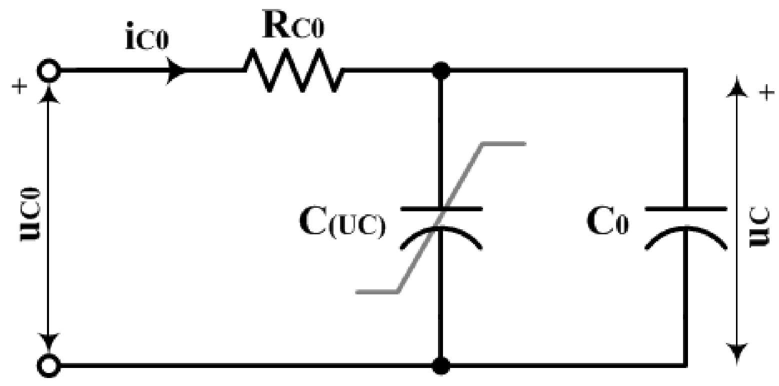
Simplified Model

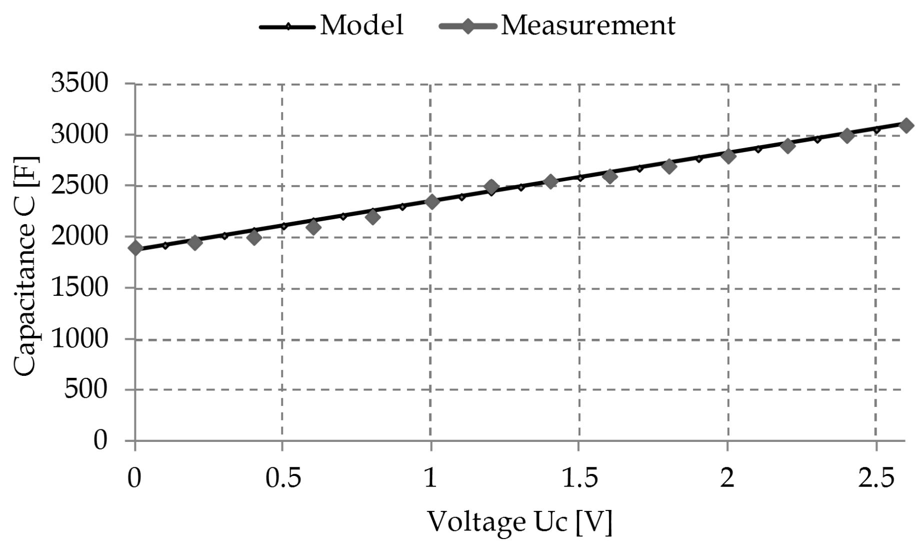
- First order nonlinear RC model
  - ESR R_{C0} is assumed constant
  - The capacitance is voltage dependen

$$C(u_C) = C_0 + k_C \cdot u_C$$

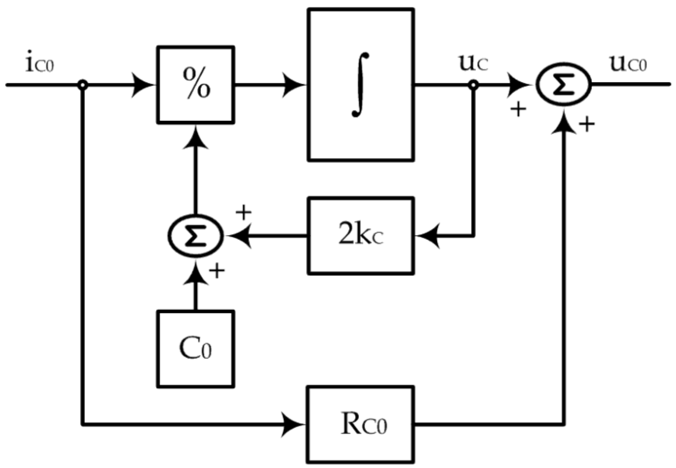
- The ultra-capacitor current

$$i_C = \frac{\partial Q}{\partial t} = \left(C(u_C) + u_C \frac{dC(u_C)}{du_C} \right) \frac{du_C}{dt} = C_I(u_C) \frac{du_C}{dt}$$

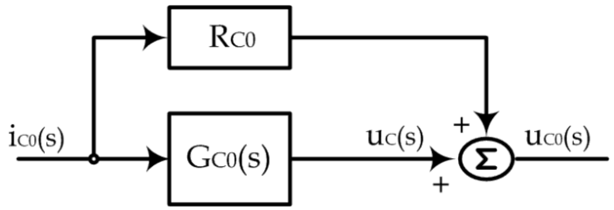




Simulation/Control Model



Large Signal (Nonlinear) Model



Small Signal (Linear) Model

$$\frac{du_C}{dt} = i_C \frac{1}{\left(C_0 + 2k_C \cdot u_C\right)}$$

$$u_{C0} = u_C + R_{C0} i_{C0}$$

$$\frac{d\hat{u}_C}{dt} = \frac{1}{\left(C_0 + 2k_C U_C\right)} \hat{i}_{C0} - \frac{2k_C I_{C0}}{\left(C_0 + 2k_C U_C\right)^2} \hat{u}_C$$

$$\hat{u}_{C0} = \hat{u}_C + R_{C0} \hat{i}_{C0}$$

Ultra-capacitor Energy Capability

- Stored Energy

$$E_C(u_C)=\frac{1}{2}\left(C_0+\frac{4}{3}k_C u_C\right)u_C^2=\frac{1}{2}C_E(u_C)u_C^2$$

- "Energetic" Equivalent Capacitance

$$C_E(u_C)=\left(C_0+\frac{4}{3}k_C u_C\right)$$

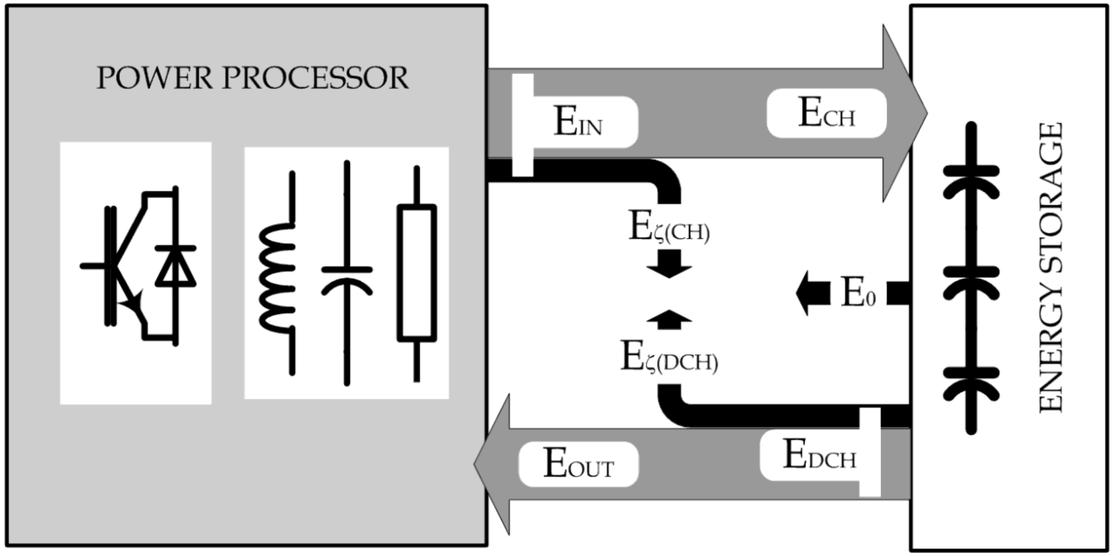
- Energy realized to the load

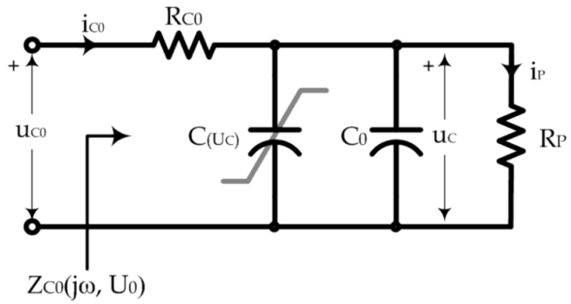
$$E_{C0}=\Delta E_C-E_{LOSSES}$$
$$=\frac{C_0}{2}\left(U_{C\max}^2-U_{C\min}^2\right)+\frac{2}{3}k_C\left(U_{C\max}^3-U_{C\min}^3\right)-\int_0^{T_{DCH}}R_{C0}(t)i_{C0}^2(t)dt$$

- Specific Energy

$$SE_C(u_C)=\frac{\left(C_0+\frac{4}{3}k_C u_C\right)u_C^2}{2M}$$

Ultra-capacitor Energy Efficiency





Charging / Discharge Efficiency

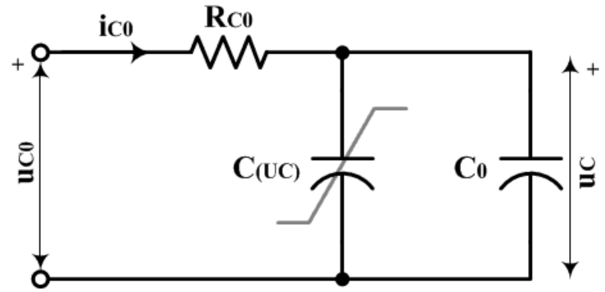
$$\eta_{CH} = \frac{E_{IN} - E_{\varsigma(CH)}}{E_{IN}} = \frac{E_{CH}}{E_{CH} + E_{\varsigma(CH)}}$$

$$\eta_{DCH} = \frac{E_{OUT}}{E_{OUT} + E_{\varsigma(DCH)}} = \frac{E_{DCH} - E_{\varsigma(DCH)}}{E_{DCH}}$$

Round Trip Efficiency

$$\eta_{RTP} = \frac{E_{OUT}}{E_{IN}} = \frac{E_{DCH} - E_{\varsigma(DCH)}}{E_{CH} + E_{\varsigma(CH)}} = \frac{E_{CH} - E_0 - E_{\varsigma(DCH)}}{E_{CH} + E_{\varsigma(CH)}}$$

Ultra-capacitor Power & Current



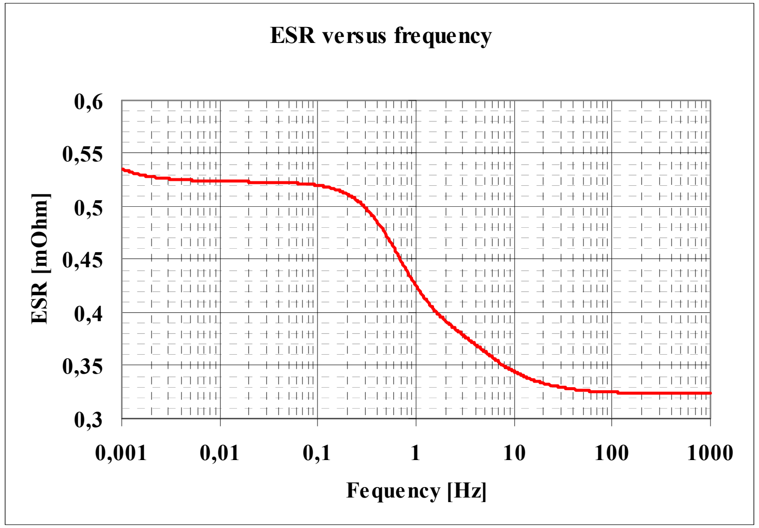
- Maximum Power $$P_{0MAX} = \frac{u_C^2}{4R_{C0}}$$
- Maximum Power IEC 62391-2 $$P_{0(D)} = 0.12\frac{u_C^2}{R_{C0}}$$
- Maximum Specific Power $$SP_{0\max} = \frac{u_C^2}{4R_{C0}M}$$
- Maximum Specific Power IEC 62391-2 $$SP_{0(D)} = 0.12\frac{u_C^2}{R_{C0}M}$$
- Maximum 1s Current $$I_{\max} = \frac{1}{2}\frac{u_C C_0}{(C_0 R_{C0} + 1)}$$
- Carbon Loading Capability $$I_{\max(CL)} = C_0 k_{CL}$$

Frequency Dependent Losses

- ESR R_{C0} depends on frequency
- Consider steady state operating voltage U_0
  - The system is linear (linearized)
  - However $R_{C0} = R_{C0}(\omega)$ $R_{C0} = R_{C0}(t)$

$$u_{ESR}(t) \neq R_{C0} \cdot i_{C0}(t)$$

$$i_{C0}(t) = I_{C0}\sin(\omega_0 t)$$



The capacitance C_0=2500F at operating point U_0=1V. Nominal voltage U_{C0}=2.5V

- If the current is sinusoidal
  - Instantaneous terminal voltage and power

$$u_{ESR}(t) = U_{ESR}\sin(\omega_0 t) = R_{C0}(\omega)\big|_{\omega=\omega_0} I_{C0}\sin(\omega_0 t) = R_{C0}(\omega)\big|_{\omega=\omega_0} i_{C0}(t)$$

$$p(t) = u_{ESR}(t) \cdot i_{C0}(t) = f(i_{C0}(t)) \cdot i_{C0}(t)$$

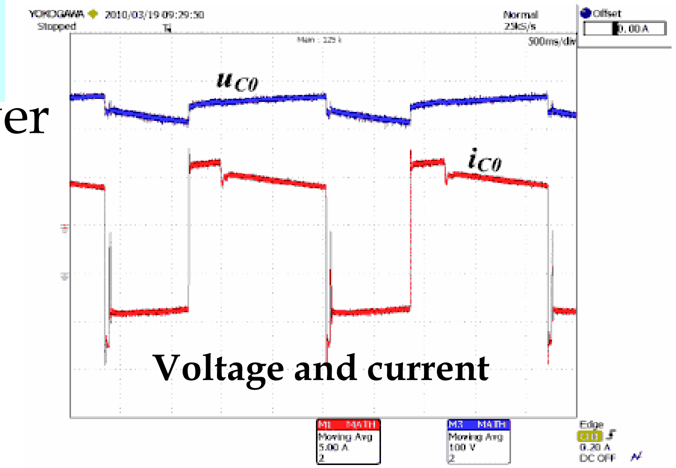
Frequency Dependent Losses

Case A:

- The current is periodic $i_{C0}(t)=\sum_{k=0}^{+\infty} I_{C0(k)} \sin(k\omega_0 t + \varphi_k)$
- The terminal voltage and instantaneous power

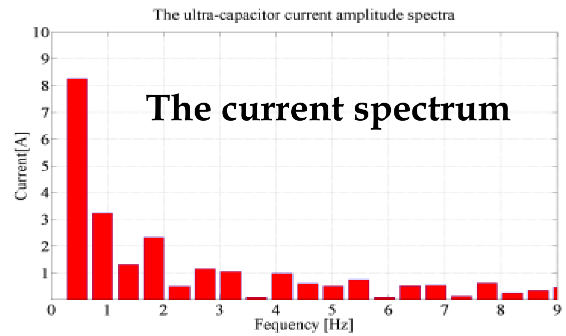
$$u_{ESR}(t)=\sum_{k=0}^{+\infty} R_{C0}(k\omega_0)\cdot I_{C0(k)} \sin(k\omega_0 t + \psi_k)$$

$$p(t)=\sum_{k=0}^{+\infty} I_{C0(k)} \sin(k\omega_0 t + \varphi_k)\cdot \sum_{k=0}^{+\infty} R_{C0}(k\omega_0) I_{C0(k)} \sin(k\omega_0 t + \varphi_k)$$



- Average power P_{AV} over a period T

$$P_{AV}(T)=\frac{1}{2}\sum_{k=0}^{+\infty} R_{C0}(k\omega_0)\cdot I_{0(k)}^2$$



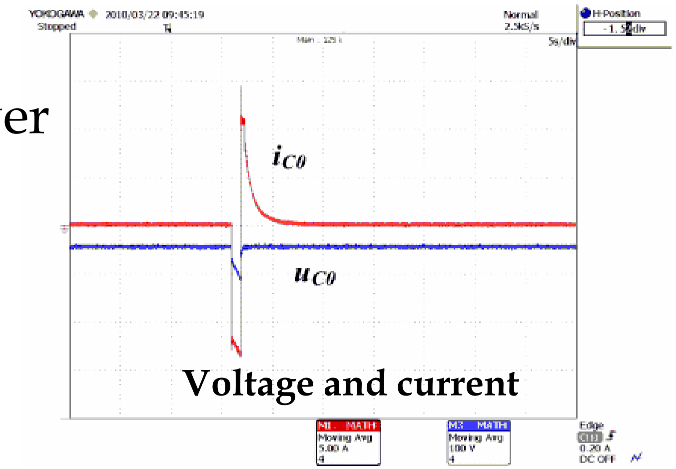
Frequency Dependent Losses

Case B:

- The current is not periodic $i_0(t) = \frac{1}{2\pi}\int_{-\infty}^{+\infty} I(j\omega)e^{j\omega t}\,d\omega$.
- The terminal voltage and instantaneous power

$$u_{ESR}(t) = \frac{1}{2\pi}\int_{-\infty}^{+\infty} R_{C0}(j\omega) I(j\omega)e^{j\omega t}\,d\omega$$

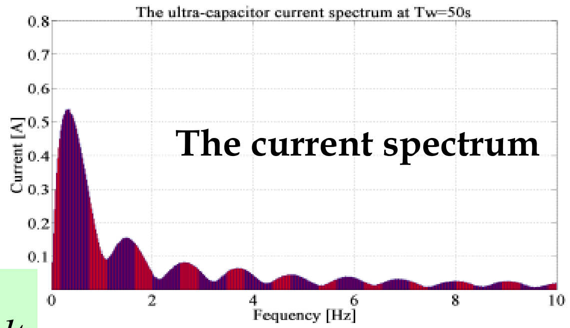
$$p(t) = \frac{1}{4\pi^2}\int_{-\infty}^{+\infty} I(j\omega)e^{j\omega t}\,d\omega \cdot \int_{-\infty}^{+\infty} R_{C0}(j\omega) I(j\omega)e^{j\omega t}\,d\omega$$



- Energy E_{ESR} determines the ultra-capacitor thermal image

$$P_{AV} = \lim_{T\to\infty}\frac{1}{T}\int_{-\frac{T}{2}}^{+\frac{T}{2}} p(t)\,dt = 0$$

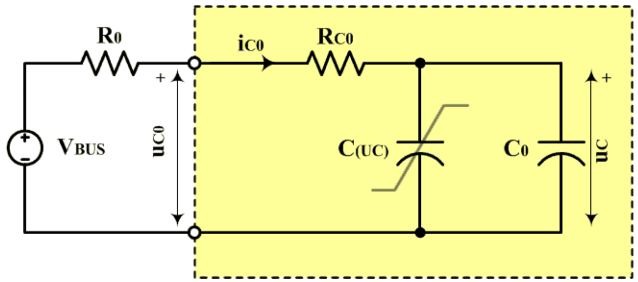
$$E_{RESR} = \int_{-\infty}^{\infty} p(t)\,dt = \frac{1}{4\pi^2}\int_{-\infty}^{\infty}\left(\int_{-\infty}^{+\infty} I(j\omega)e^{j\omega t}\,d\omega \cdot \int_{-\infty}^{+\infty} R_{C0}(j\omega) I(j\omega)e^{j\omega t}\,d\omega\right)dt$$



Charge and Discharge Methodes

1. **Constant voltage**

- The ultra-capacitor charge/discharged from/to voltage V_{BUS} via a resistor R_0
- The resistor is **must**, but not practical
  - Low efficiency



Constant voltage charge/discharge circuit

2. **Constant current**

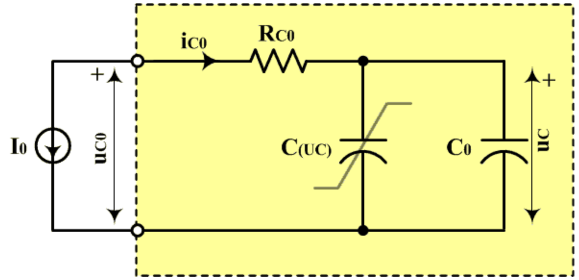
- Very common method in applications
- Maximum discharge power and current

$$P_{0MAX} = \frac{u_C^2}{4R_{C0}} \qquad I_{0MAX} = \frac{u_C}{R_{C0}}$$

- Maximum charge power and current

$$P_{0MAX} = \frac{U_{0\max}\left(U_{0\max} - u_C\right)}{R_{C0}} \qquad I_{0MAX} = \frac{U_{0MAX} - u_C}{R_{C0}}$$

  - limited by the current source terminal voltage U_{0max}

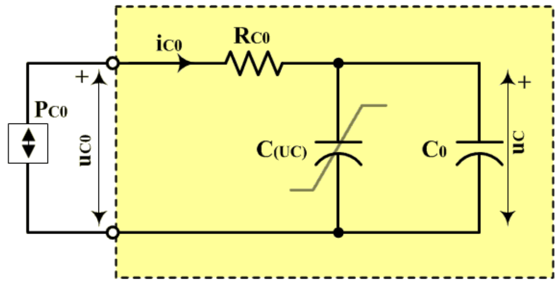


Constant current charge/discharge circuit

Charge and Discharge Methodes

3. Constant power

- The most common method in applications
- Maximum discharge power
- $$P_{0MAX} = \frac{u_C^2}{4R_{C0}}$$



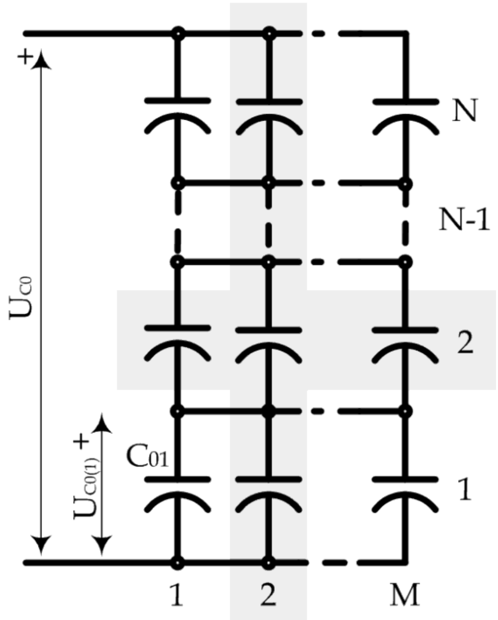
Constant power charge circuit

- If the power source exceeds maximum power, the voltage will collapse
- Maximum charge power is limited by the power source terminal voltage $$P_{0MAX} = \frac{U_{0\max}\left(U_{0\max} - u_C\right)}{R_{C0}}$$
- Charge/discharge current (resistance R_{C0} is neglected)

$$i_{C0} \cong \pm \frac{|P_{C0}|}{U_C}\sqrt{\frac{C_0 U_C^2}{C_0 U_C^2 \pm 2P_{C0}t}}$$

Ultra-capacitor Modules

- Cell voltage is very low, not practical for power conversion application
- N cells are series connected in a module,
- M cells are parallel connected

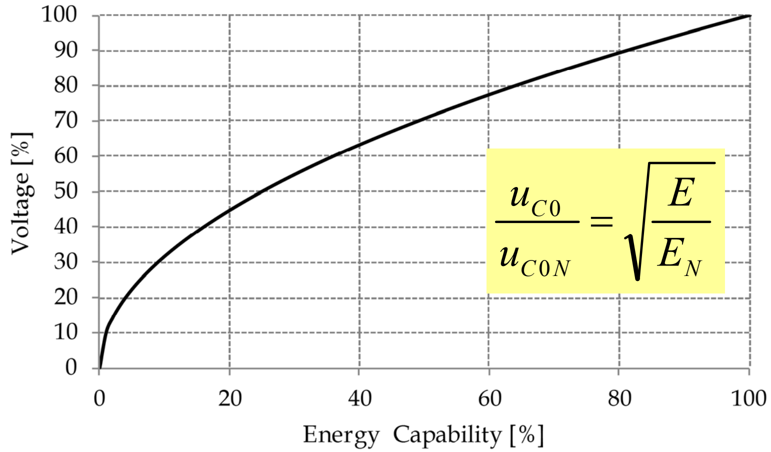


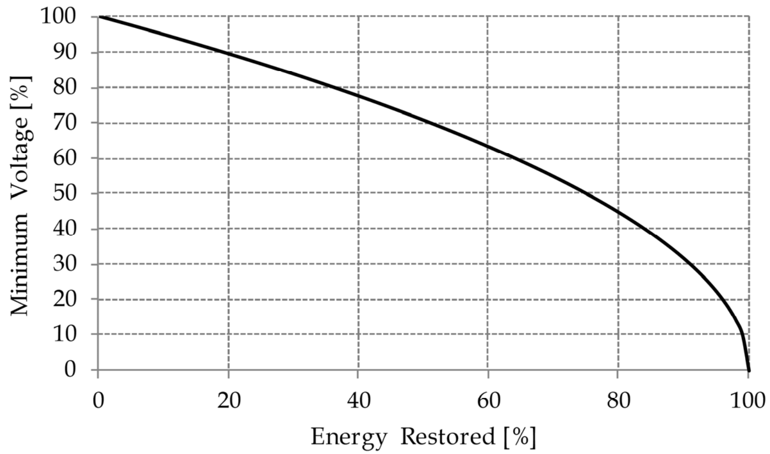
Ultra-capacitor Modules

Module	Voltage [V]	Capacitance [F]	SE [Wh/kg]	Weight [kg]
Maxwell Technologies				
BMOD0500	16	500	3.2	5.51
BMOD0083	48	83	2.6	10.3
BMOD0130	56	130	3.1	18
BMOD0094 P075	75	94	2.9	25
BMOD0063 P125	125	63	2.3	65
LS MTRON Ultra-capacitors				
LS 16.2V / 500F	16.2	500	3.5	5.1
LS 33.6V/250F	33.6	250	4	9.8
LS 50.4V/167F	50.6	166	3.43	17.2
LS 201.6V/41F	201.1	41	2.21	104

Integration of ES into the System

- The ultra-capacitor voltage varies with the state of charge (SOC)
- If the ultra-capacitor is directly connected
    1. The ultra-capacitor is oversized
        - Not cost and size effective
    2. The conversion system voltage rating is N+1
        - Not cost effective
        - Efficiency issue
- Not convenient to directly connect the ultra-capacitor to the conversion system



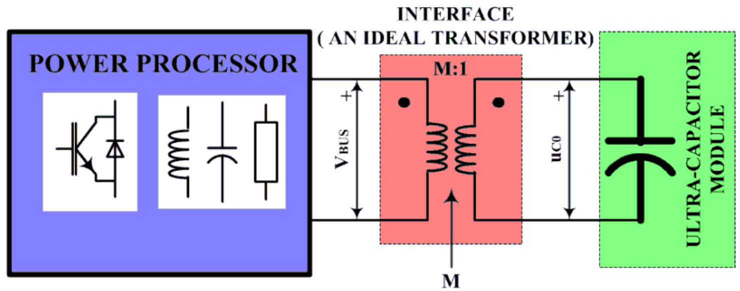


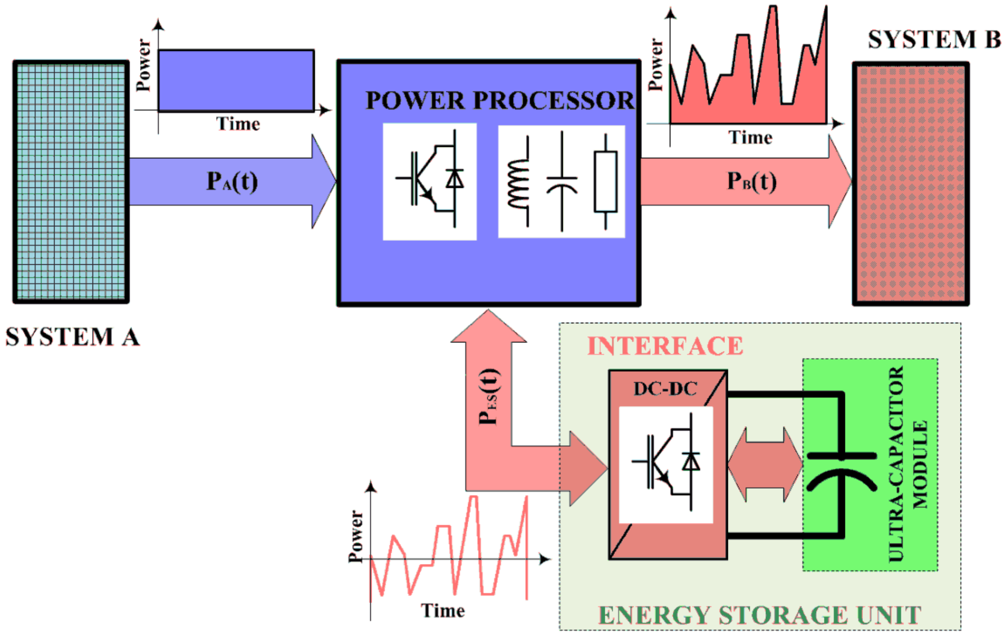
Integration of ES into the System

- The ultra-capacitor voltage has to be matched with the power processor dc bus voltage V_{BUS}
- An ideal transformer with variable gain M

$$M = \frac{V_{BUS}}{u_{C0}} = \frac{const}{u_{C0}}$$

- Bidirectional "Loss-free" dc-dc converter emulates an ideal transformer
- Topology of dc-dc converter in numerous variety





The Ultra-capacitors of Future

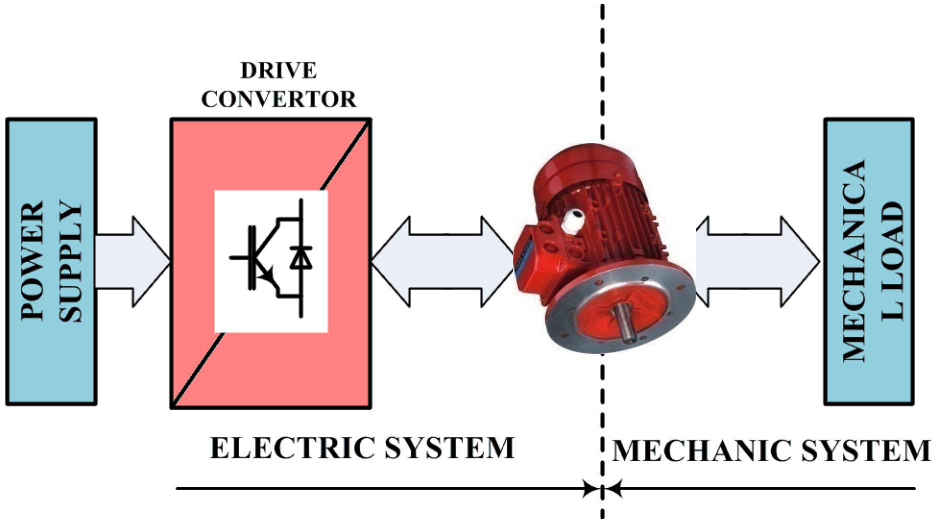
1. Energy density at least x10 of the existing (50Wh/kg to 100Wh/kg)
2. Lower internal resistance, <50% of existing
   - Higher power density
3. Higher cell voltage
   - Lower number of series connected cells into a string, higher reliability
4. Self balancing capability
   - No need for an external balancing circuit, lower complexity, lower cost, higher reliability
5. Higher operating temperature
   - >85^{o}C, >10 years life time
6. Strongly voltage dependent capacitance (Voltage-SOC characteristic)
   - Smaller variation of the terminal voltage
   - Higher minimum discharge voltage , lower current rating, smaller interface dc-dc converter

PART THREE
Applications

1. Controlled electric drives
2. Renewable energy
3. Diesel electric generators
4. STATCOM and power quality
5. UPS
6. Traction drives

App 1: Controlled Electric Drives

- Electric drives convert electric energy into mechanical energy
  - Move an object
- > 60% of total electricity production is consumed by electric drives
- Numerous applications
  1. Hoisting and lift applications
  2. Machines with intermittent load
  3. Blowers and Pumps
  4. Traction drives
  5. Home appliance drives

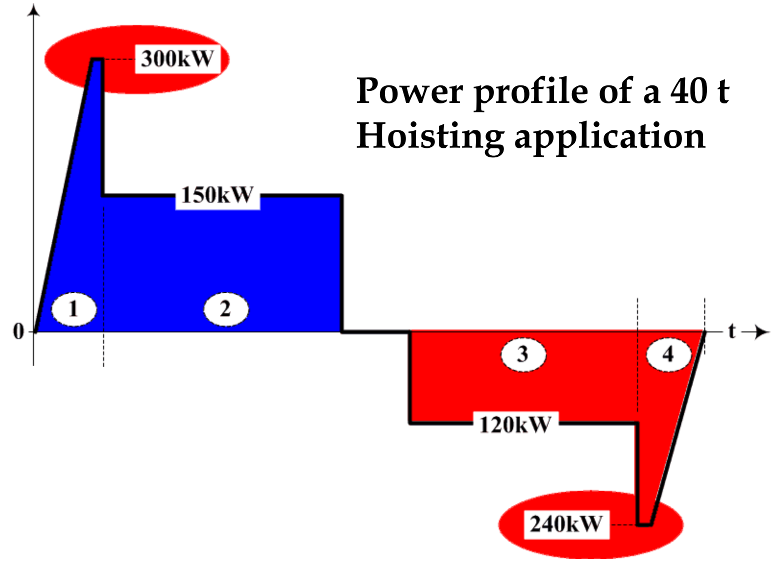


❖ **The project "Application of ultra-capacitors in controlled electric drives" was sponsored by Schneider Toshiba Inverter, Pacy sur Eure, Franca and the Laboratoire d'Électrotechnique et d'Électronique de Puissance de Lille, l'Ecole Centrale de Lille, Villeneuve d'Ascq, France from 2007 until 2010.**

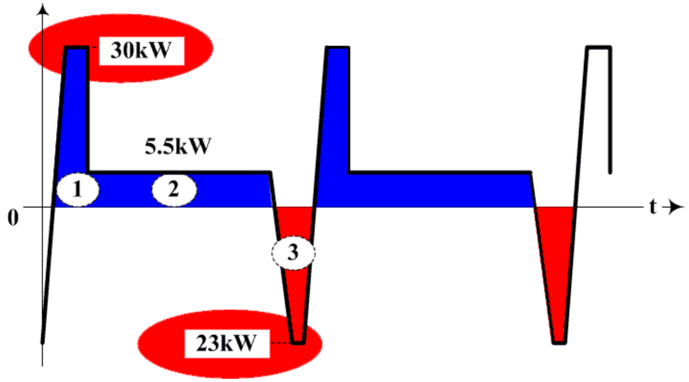
App 1: Controlled Electric Drives

Application issues

1. Braking energy
   - Dissipated on a brake resistor
   - 25 to 40% of consumed energy
2. Ride through capability
   - Critical in certain applications
   - 10kE up to 1ME per interruption
   - Ride through time up to 10 to 15s
3. High ratio of peak to average power
   - Peak power penalties
   - The installation size and cost
   - Voltage fluctuation and flickers



Power profile of a 40 t Hoisting application

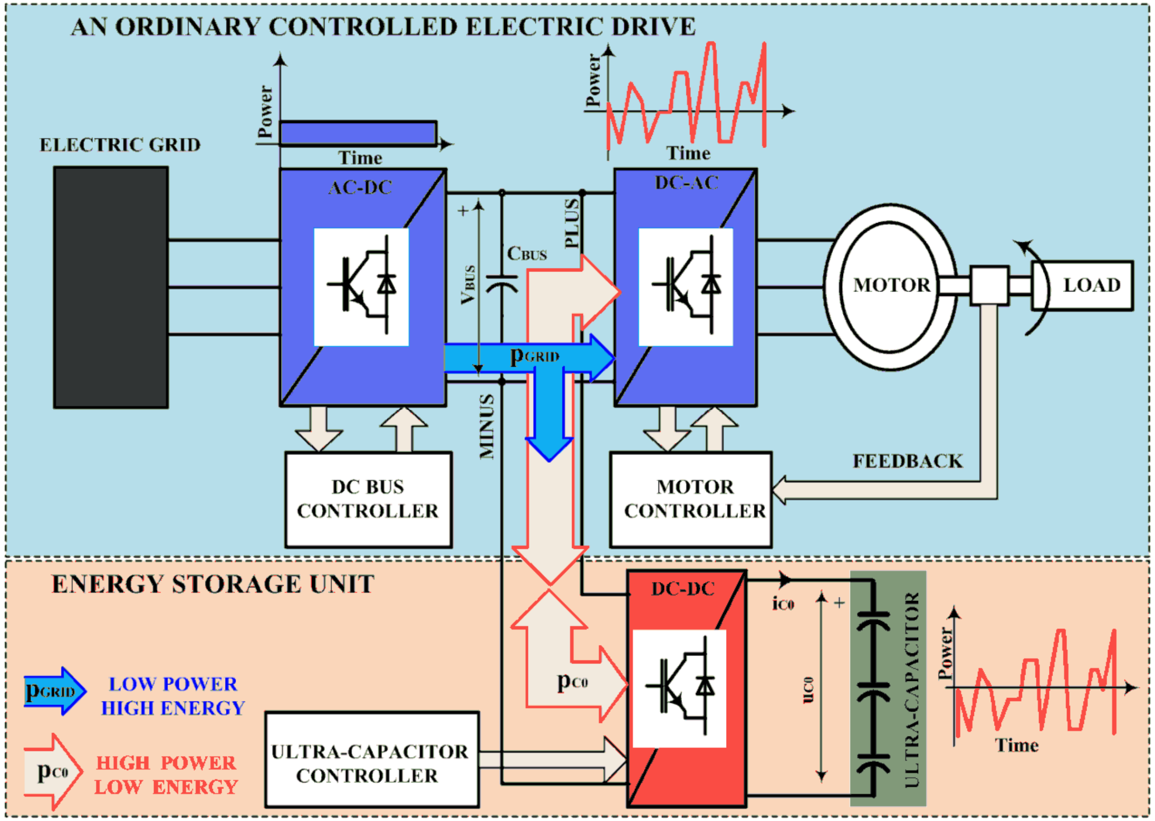


Power profile of an intermittent load VSD

App 1: Controlled Electric Drives

A controlled electric drive with an ultra-capacitor as energy storage

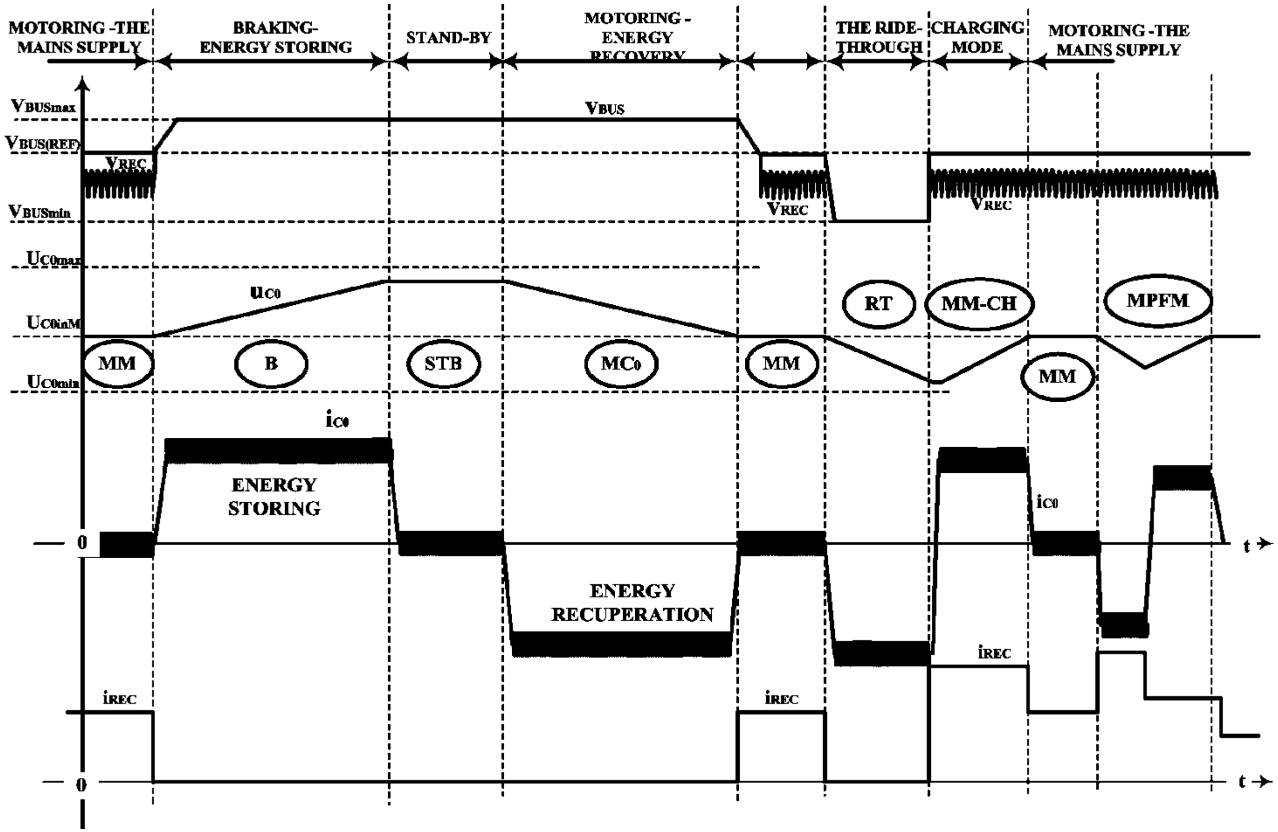
- Ultra-capacitor energy storage
  - To store and restore the drive braking energy
  - Low voltage ride through capability
  - To smooth the drive power
- The ultra-capacitor is controlled independently from the motor control
  - As an option



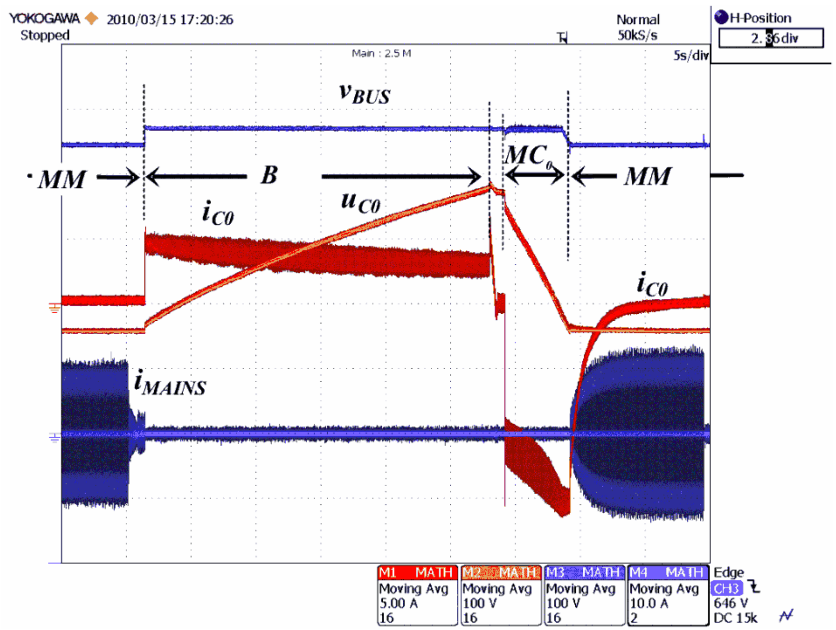
App 1: Controlled Electric Drives

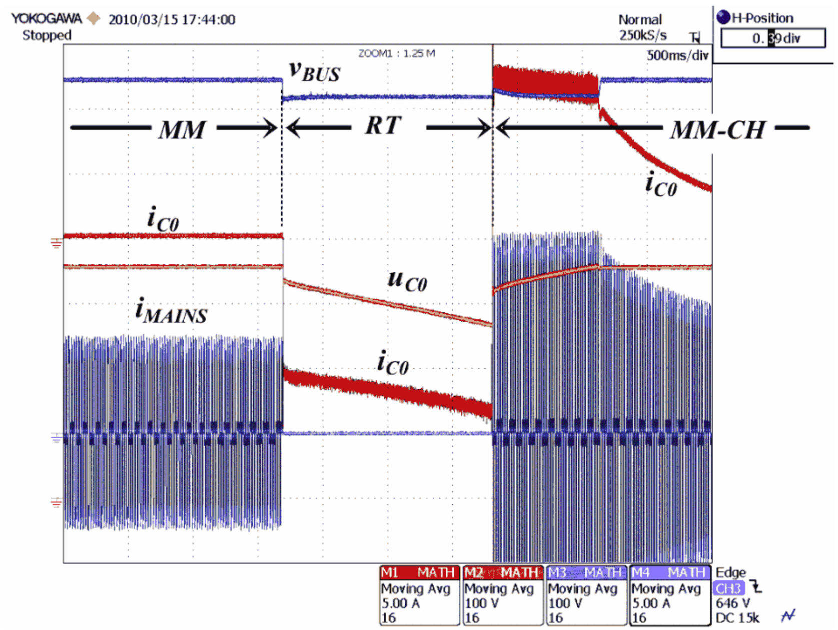
Basic operating modes

- **MM**: The mains motoring
- **B**:Braking
- **STB**: Stand by
- **MC$_0$**: Energy recuperation
- **RT**: Ride through
- **MM-CH**: Mains and charging
- **MPFM**: Mains power smoothing



App 1: Controlled Electric Drives



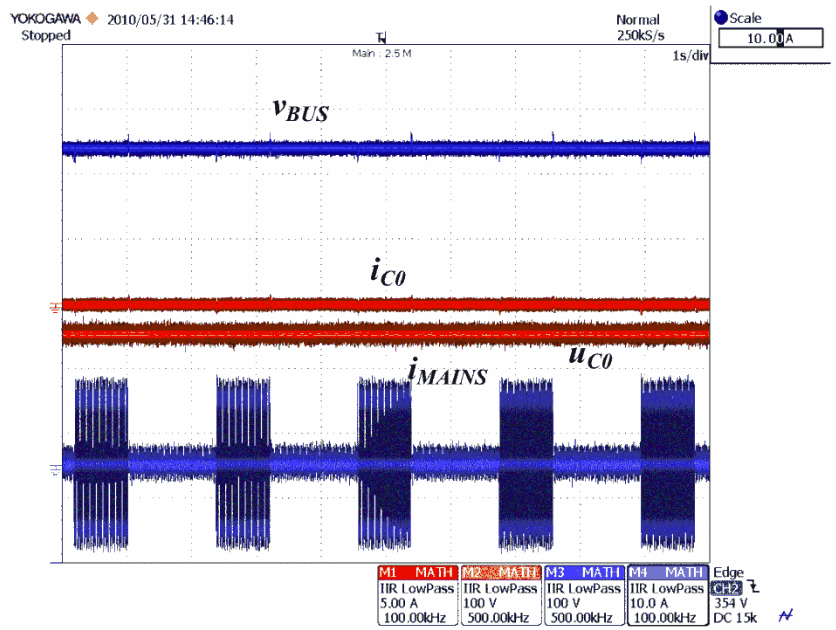


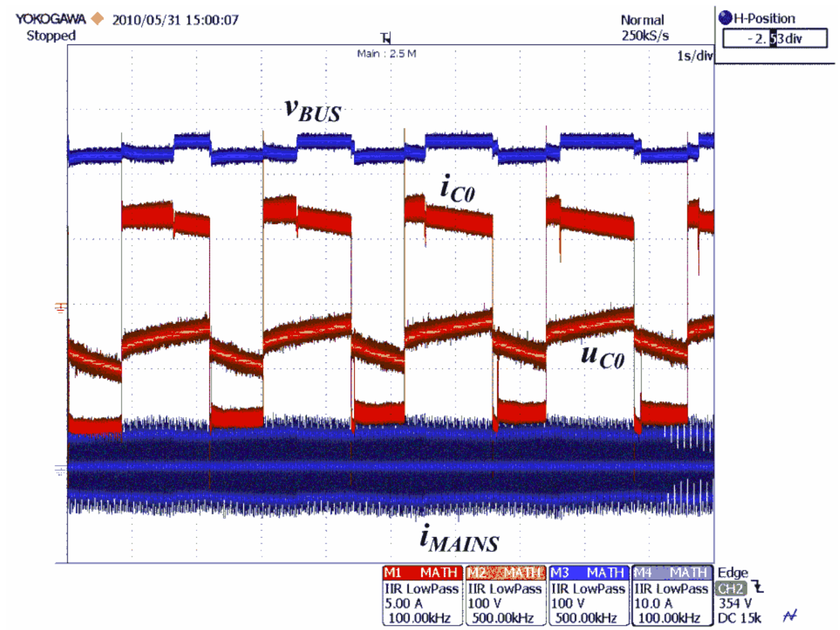
A. Braking and energy recovery

B. Low voltage ride through

Rated power P_N=5.5kW, The grid voltage V_{MAINS}=400V, dc bus voltage V_{BUS}=650V, Ultra-capacitor C_0=0.4F U_{C0}=780V

App 1: Controlled Electric Drives





A. Power smoothing function NO

B. Power smoothing function YES

Rated power P_N=5.5kW, The grid voltage V_{MAINS}=400V, dc bus voltage V_{BUS}=650V, Ultra-capacitor C_0=0.4F U_{C0}=780V

App 2: Renewable Energy

- Contribution of wind and solar renewable sources to total electricity production is dramatically increasing
- Renewable sources are connected to the grid
- The production output (power) is not constant and deterministic
  - Wind speed
  - Radiation coefficient
- Significant influence on the grid voltage and frequency regulation and the grid stability
  - Time scale of couple of seconds

www.renewablepowernews.com

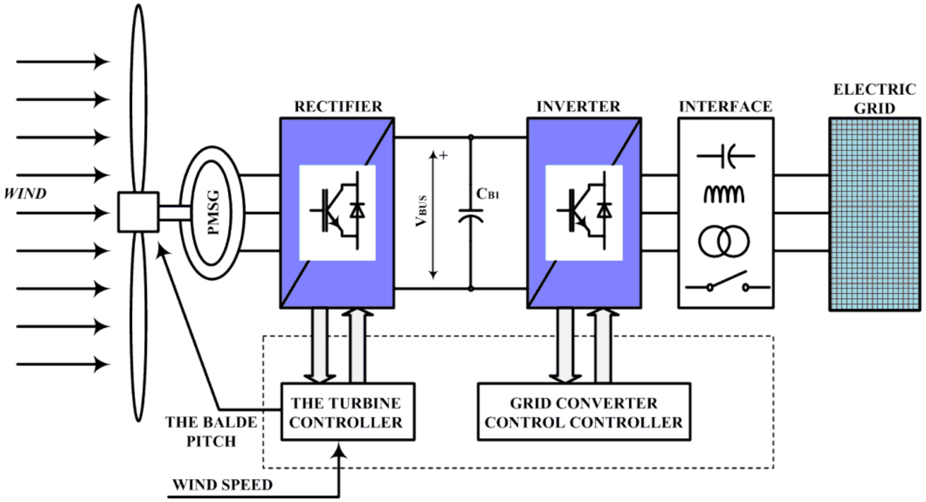
App 2: Renewable Energy

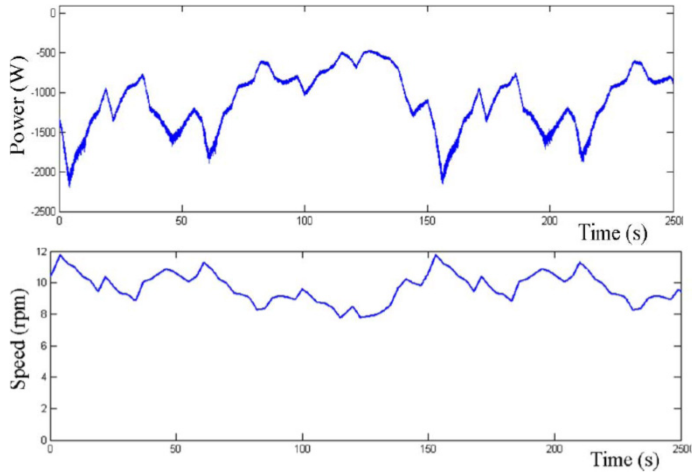
Wind Energy

- Wind speed is not constant and deterministic
- The turbine power strongly depends on the wind speed

$$P_{OUT} = C v_W^3$$

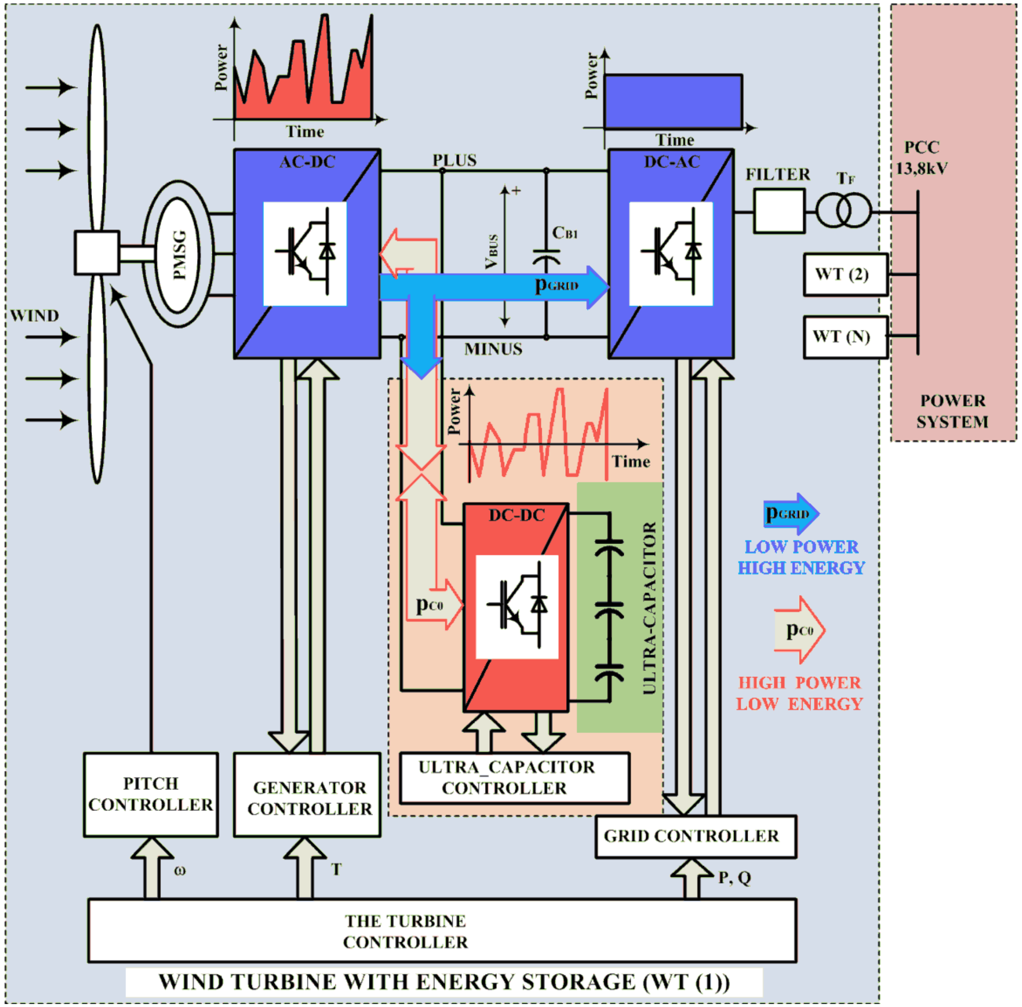
- The blade pitch
  - To control the turbine power
  - Smoothing of the wind fluctuations
  - But, not fast enough
  - The angle saturation is limitation
- A better method to filter the power fluctuations is a need





Wind speed and turbine power [9]

App 2: Renewable Energy



- Ultra-capacitor energy storage
  - To smoot the wind turbin output power

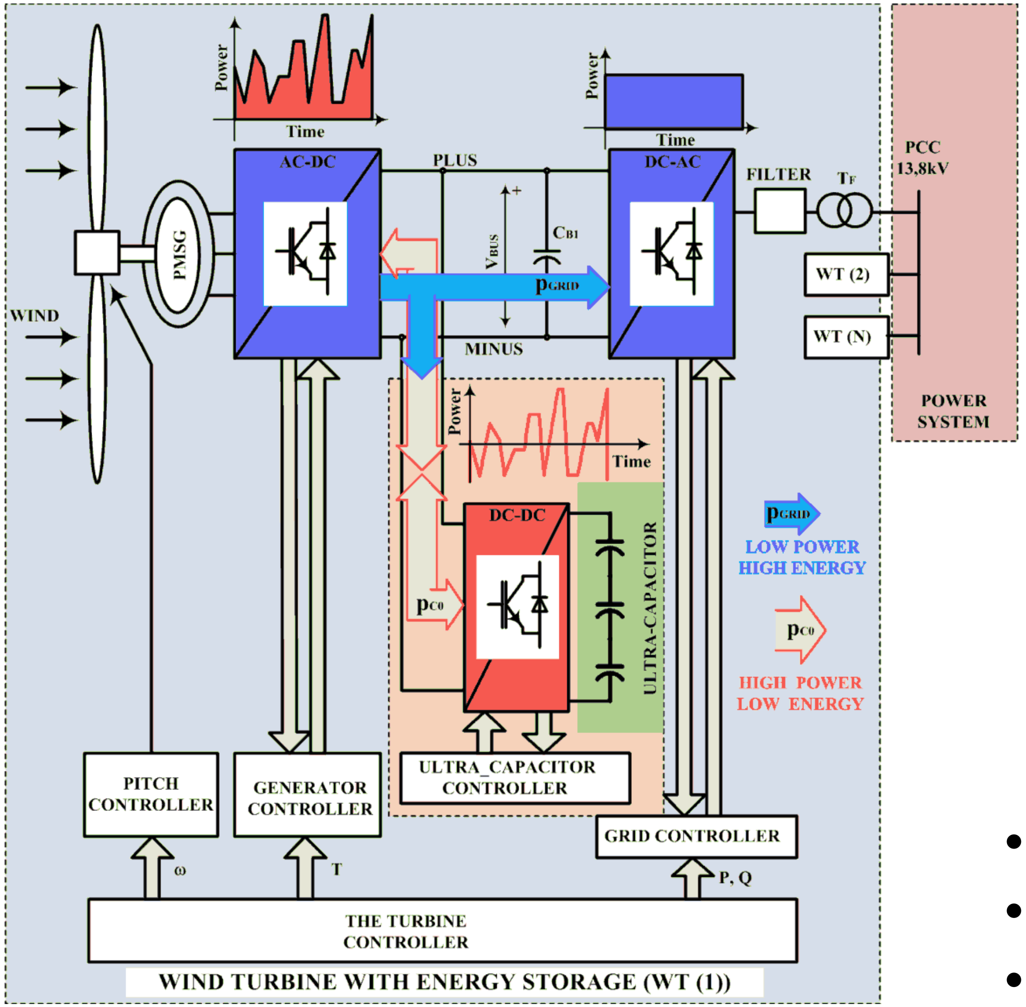
1. **Decentralized Connection**

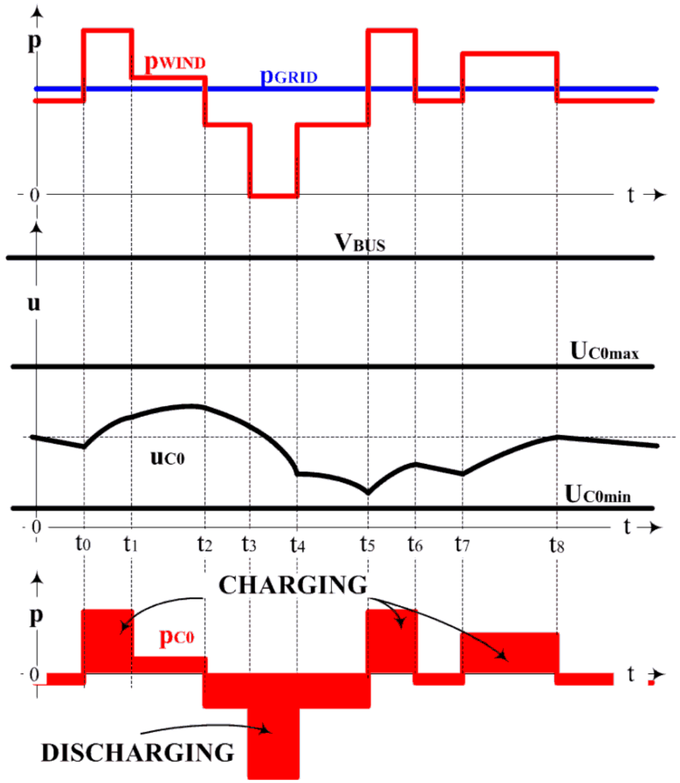
- Connected on the wind mill level
- The connection to the dc bus via an interface dc-dc converter

2. **Centralized Connection**

- Connected on the wind park (farm) level
  - Only one energy storage and interface, but
  - Increased the interface complex (AC-DC & DC-DC)
  - No redundancy

App 2: Renewable Energy





- p_{GRID} smooth
- $p_{WIND} > p_{GRID}$ Ultra-cap chargerd
- $p_{WIND} < p_{GRID}$ Ultra-cap dischargerd

App 3: Diesel Electric Generators

Energy sources used to produce electric energy from fuel, such as diesel or natural liquid gas

- Diesel electric generators are the most common solution
  - Diesel Internal Combustion Engine (ICE) drives a three-phase generator
  - The generator feeds different electric loads, motors or independent network installations

1. Rubber tyred gantry cranes (RTGC)
2. Hybrid dampers (Diesel-Electric Traction Drives)
3. Hybrid excavators
4. Autonomous diesel-electric power supplies

1

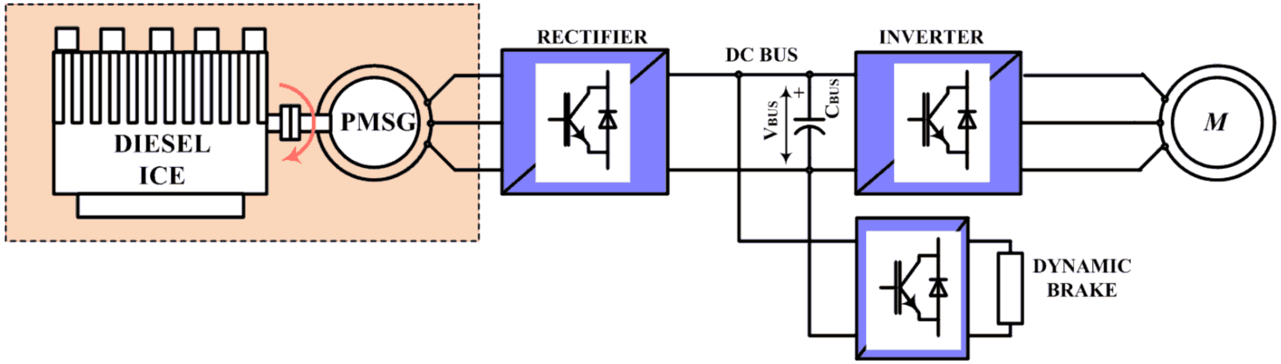
2

3

4

App 3: Diesel Electric Generators

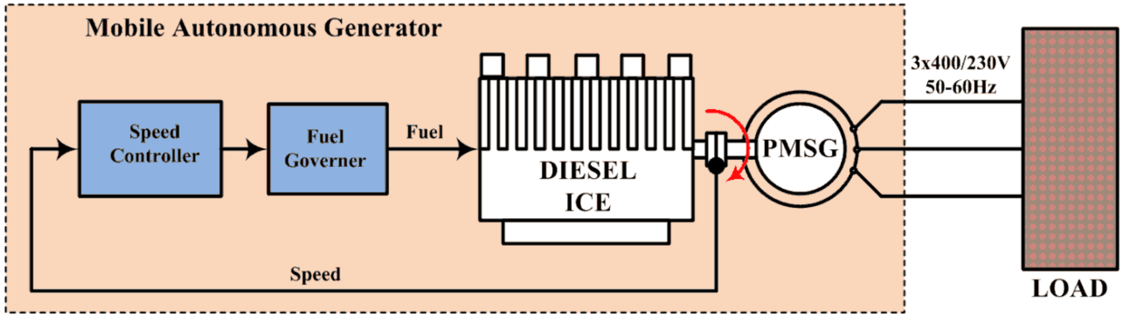
- An ICE drives a three-phase generator that feeds three-phase motor(s) via a common dc link and dislocated inverter(s)



- A brake resistor burns the drive braking energy. **An ICE is not regenerative device!**
  - 30 to 40% of consumed fuel is burned on the resistor…40t RTGC consumption of 15 to 25 [L/hour]
- Peak to average power is very high
  - The ICE sized on the peak load. The system is oversized, not cost effective

App 3: Diesel Electric Generators

- Long term UPS, Mobile generators…A Diesel ICE drives three-phase PMSG

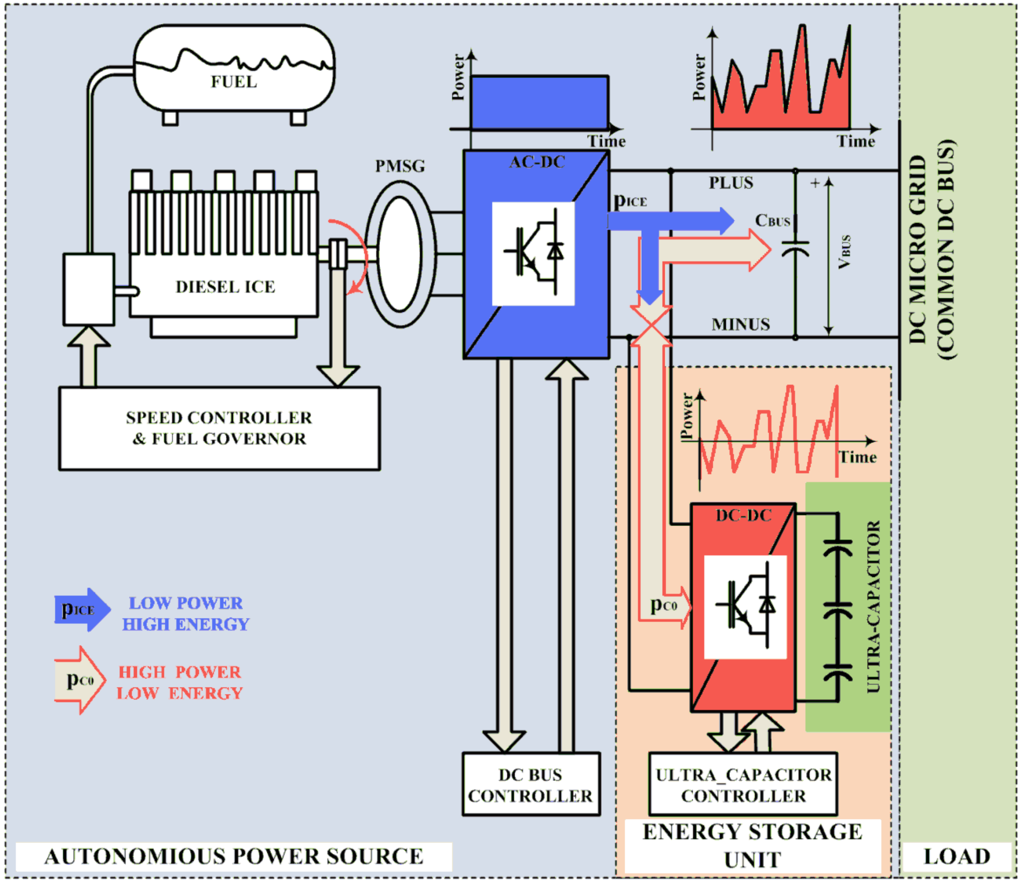


www.hardydiesel.com

- The load is directly connected to the generator
  - The output frequency and voltage must be constant ✡the generator speed has to be constant
- The engine is oversized and runs at suboptimal operating point
  - **Low efficiency, high consumption and pollution**
- The output voltage THD with nonlinear load (diode rectifier)

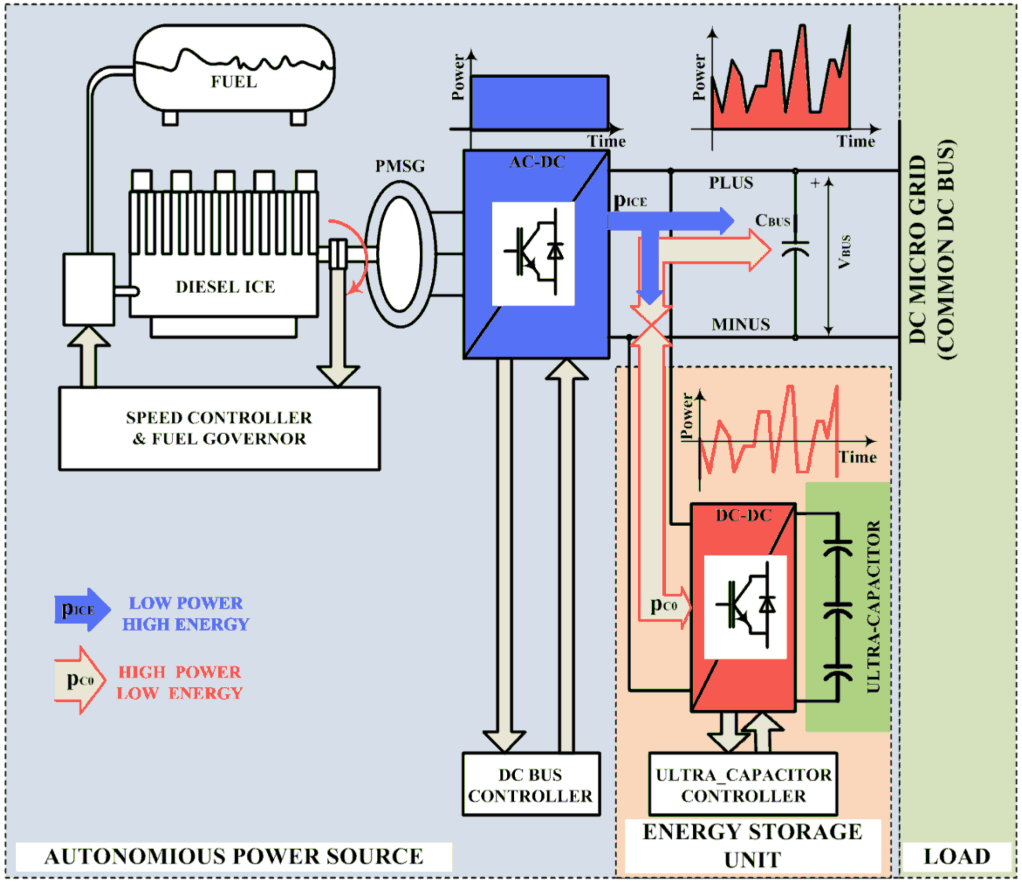
App 3: Diesel Electric Generators

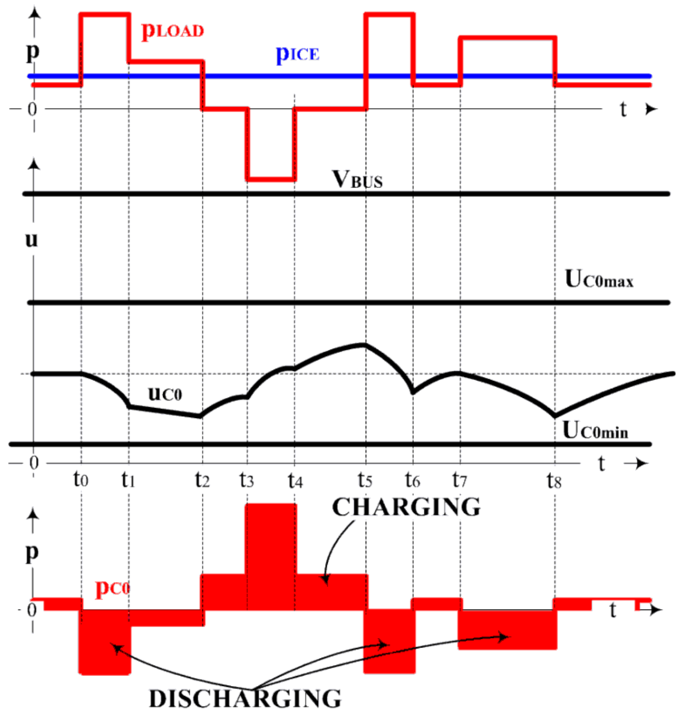
An ultra-capacitor as short term energy storage device



- All the applications have similar structure
  - A common solution can be implemented
  - Ultra-cap connected to the dc bus via a dc-dc converter
- The ultra-capacitor absorbs fluctuations of the load power
- The generator power is smooth, while the speed is variable
  - An optimal operating point.
  - Fuel saving up to 50% [10]

App 3: Diesel Electric Generators

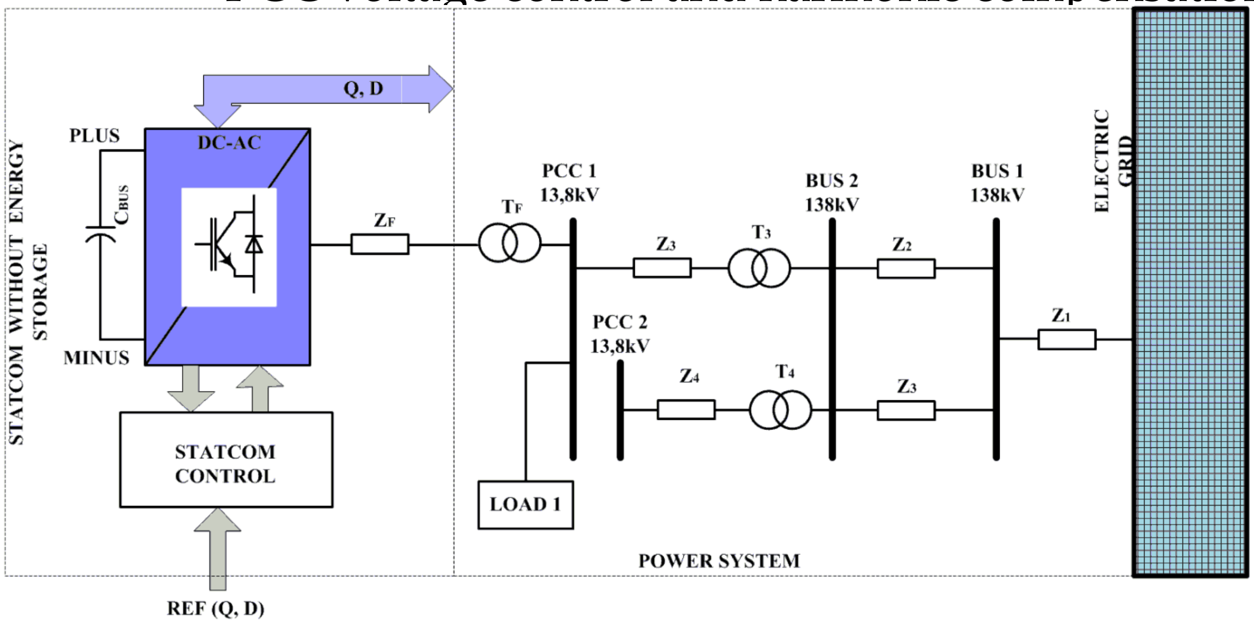


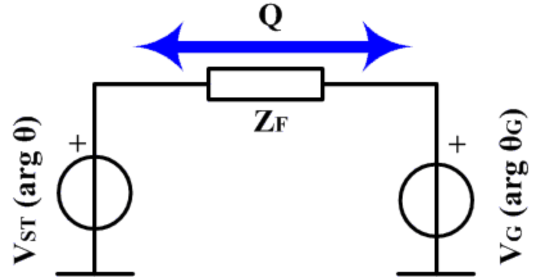


- p_{ICE} smooth function
- $p_{LOAD} > p_{ICE}$ Ultra-cap dischargerd
- $p_{LOAD} < p_{ICE}$ Ultra-cap chargerd

App 4: Power Quality

- STATic COMpensator (STATCOM) is a three-phase inverter that emulates synchronous voltage source connected to the Point of Common Coupling (PCC) of a power system
- Reactive and distortion power control
  - PCC voltage control and harmonic compensation

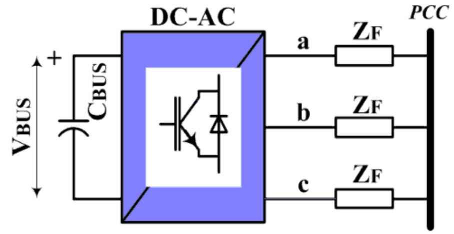


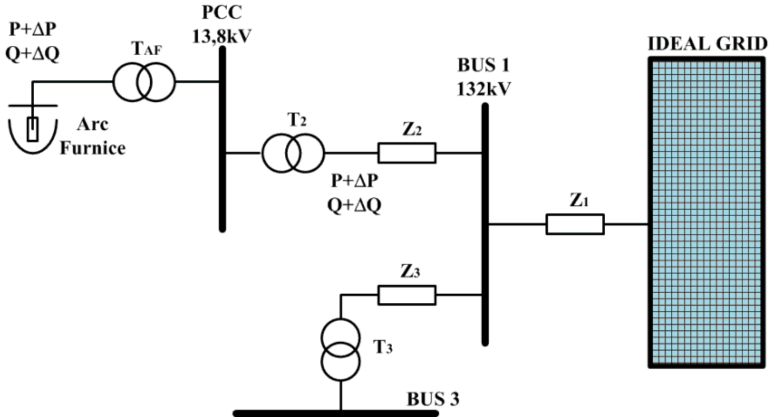


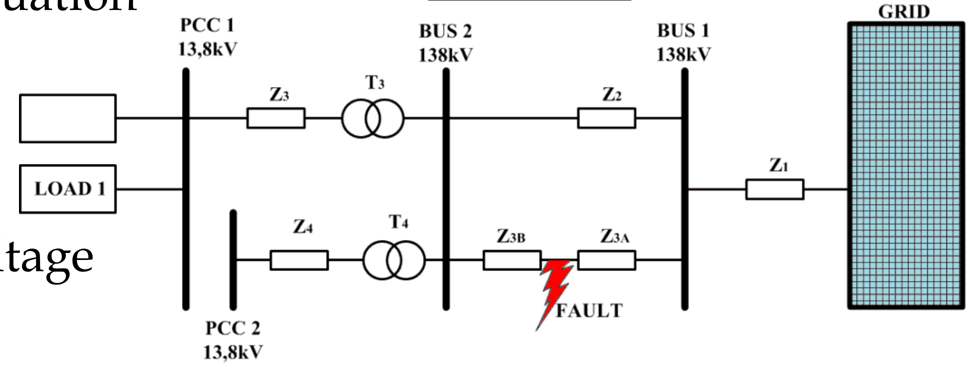
App 4: Power Quality

- The STATCOM is not a real voltage source. The dc bus is only a capacitor C_{BUS} with limited energy
  - Not possible to control active power flow on long term (<40ms)
- Some applications need active power flow control
- Arc furnaces, large drives…...
  - Smoothing active power fluctuation

1. The grid fault management
   - Handling the grid faults without significant degradation of the supply voltage power quality

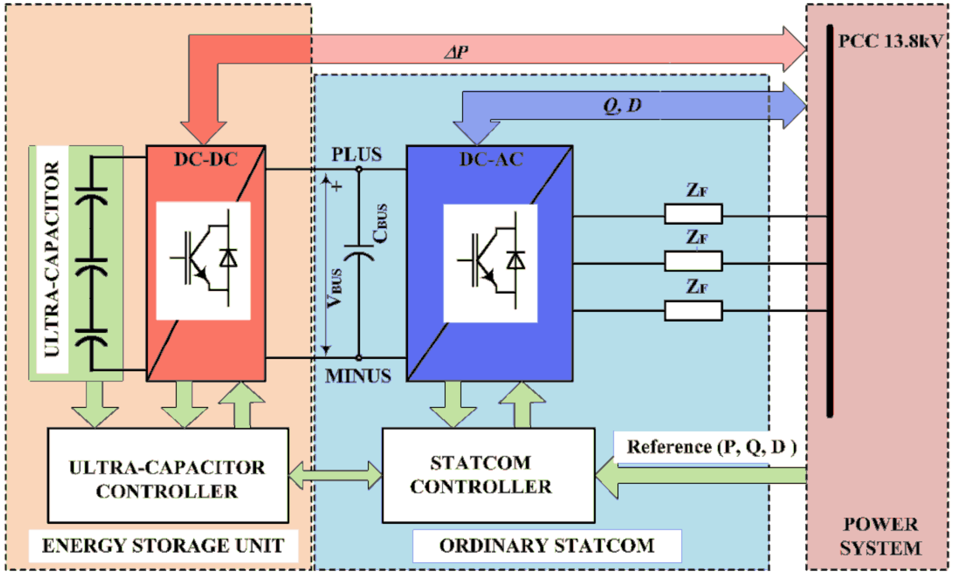


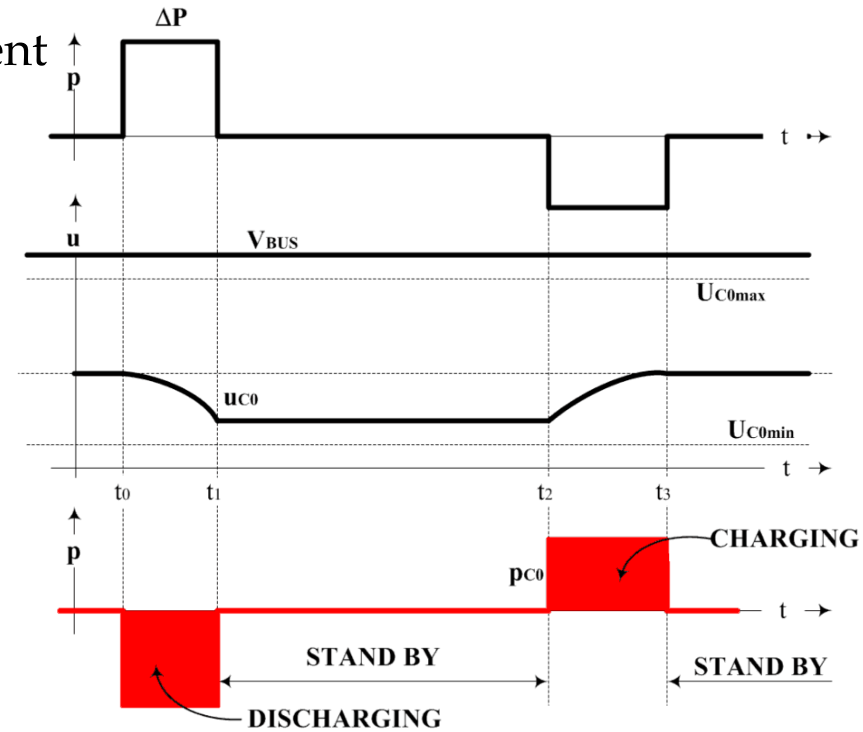




App 4: Power Quality

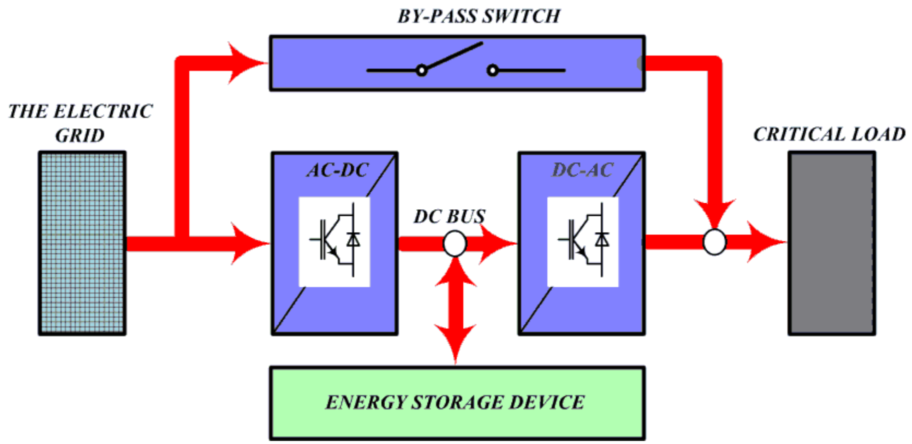
- An ordinary STATCOM equipped with ultra-capacitor energy storage
- The ultra-capacitor SOC controlled via an interface dc-dc converter
  - Dc bus voltage V_{BUS}=*const* is controlled
  - The STATCOM control is independent





App 5: UPS

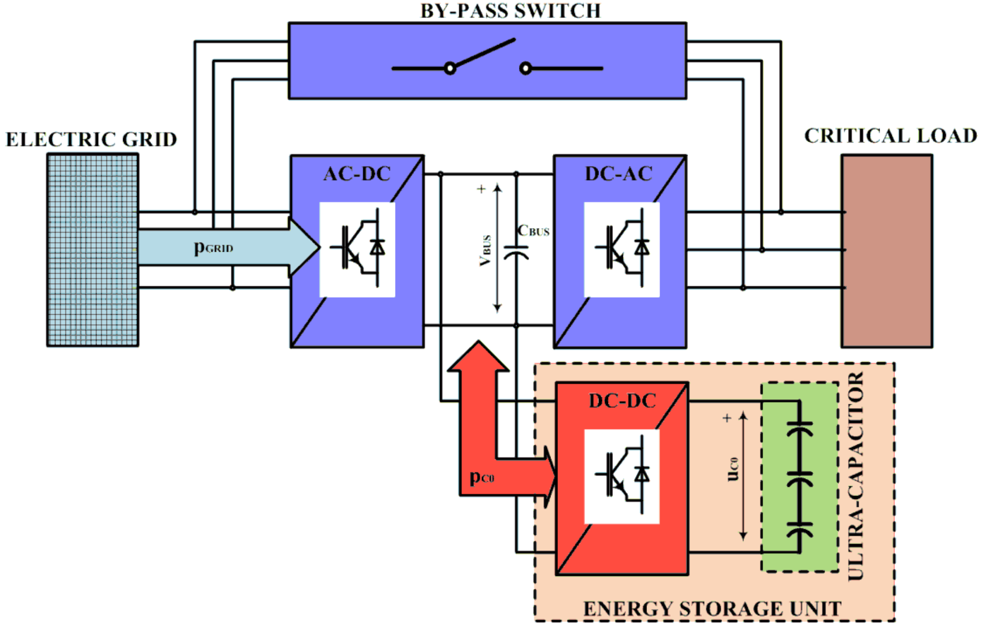
- Uninterruptible power supplies (UPS):
  - Uninterrupted, reliable, and high-quality power supply for critical loads
  - Hospitals, date centers, telecommunication and military facilities
- Static (Static power convertors + Energy storage) & Rotating (ICE & Generators
  - On-line, Off-Line & Interactive UPS
- Static UPS: Short and medium term applications, from couple of seconds up to couple of hours
- Hybrid UPS: Long term applications, up to couple of days or undefined period



App 5: UPS

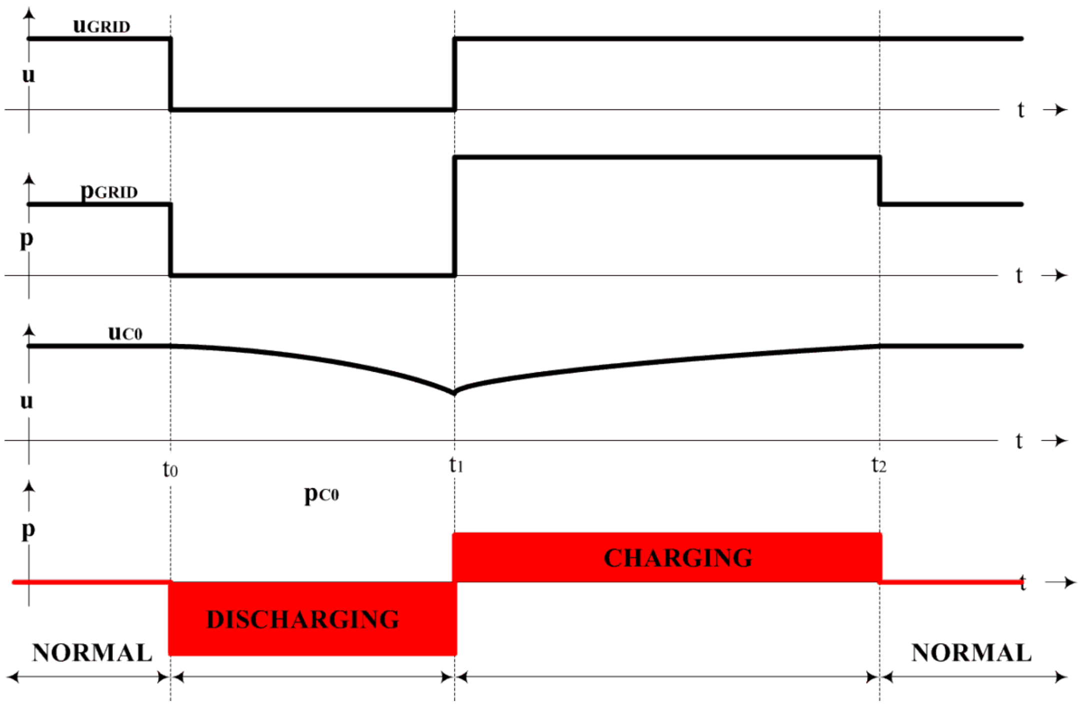
Short Term UPS Applications

- From couple of seconds up to couple of minutes
- Electrochemical batteries are still the main choice as energy storage
- The battery size is defined by the power rating not energy capability
  - Not cost effective in case of very short bridging time **(<10 to 15s)**
- The battery life time and maintenance limiting factor
- Ultra-capacitor as an alternative energy storage
  - Cost effective in case of short bridging times
  - Long life
  - Fast recharging
  - Maintenance free



App 5: UPS

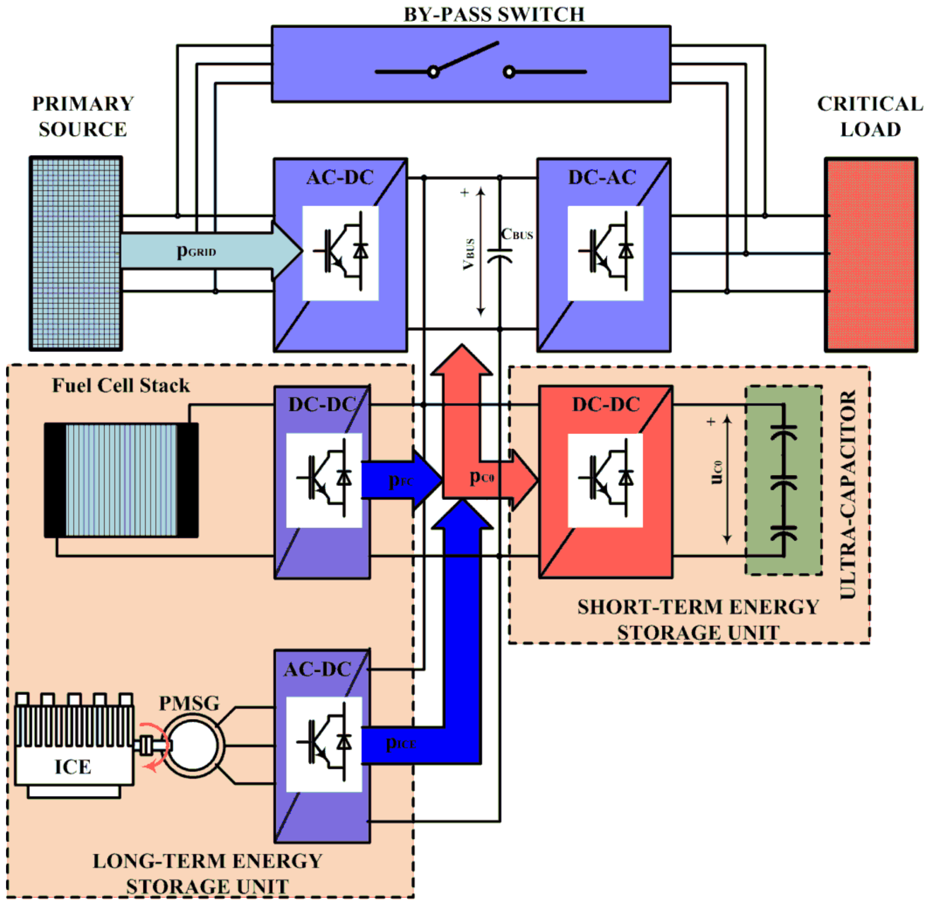
Short Term UPS Applications



App 5: UPS

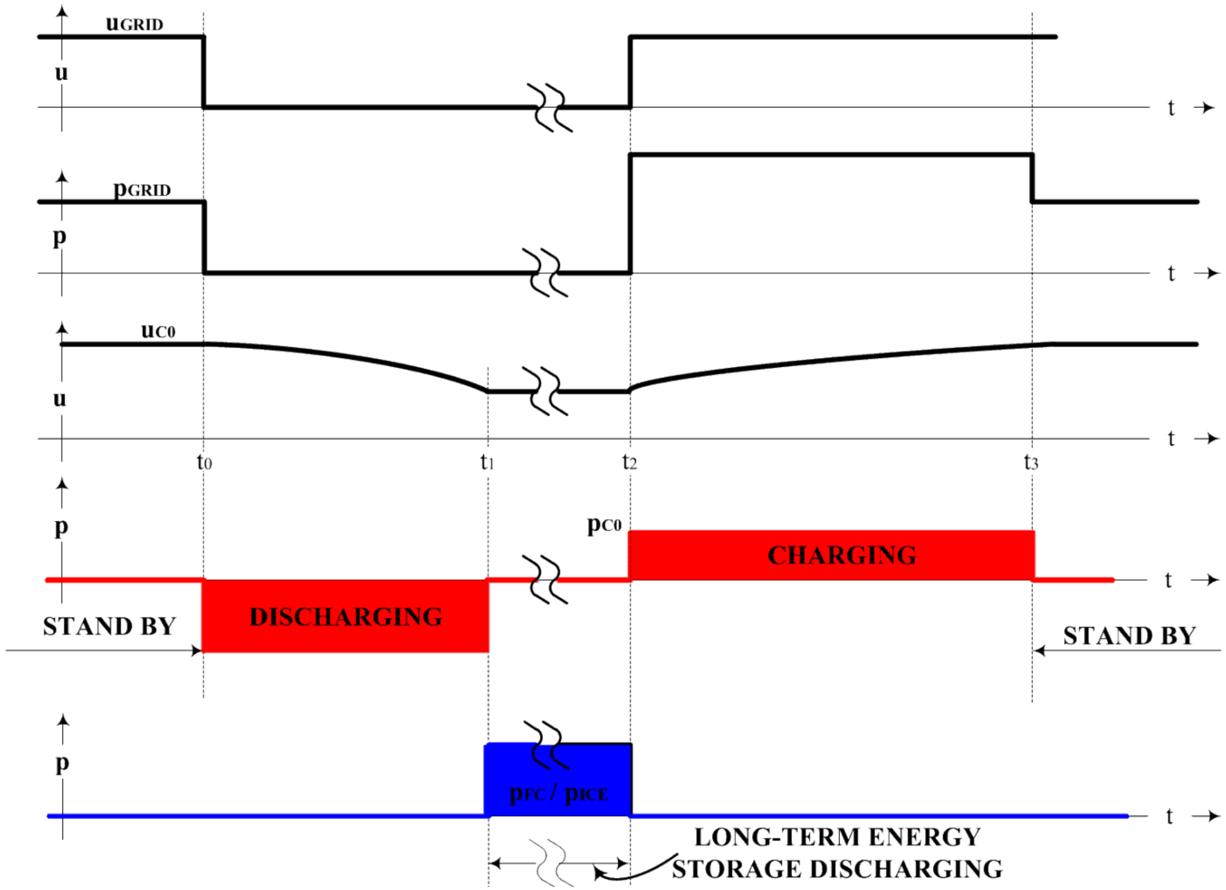
Long Term Hybrid UPS Applications

- From couple of minutes up to couple of days
- Diesel ICE or Hydrogen as energy source
  - Warming (start up) time is couple of seconds
  - An additional energy storage with fast response is the need to bridge the start up time
  - Ultra-capacitor is a candidate
  - The philosophy as short term UPS



App 5: UPS

Long Term Hybrid UPS Applications



App 6: Traction

Overview

- Rail Vehicles
  1. Heavy-rail Catenary Supplied Vehicles
  2. Heavy-rail Diesel-supplied Vehicles
  3. Light Rail Rapid Transit Vehicles
- Road Vehicles
  4. Public Transportation Catenary Supplied Vehicles,
  5. Hybrid Electric Vehicles,
  6. Electric Vehicles
- Off-Road Vehicles
  7. Heavy Tracks and Dampers

1

2

3

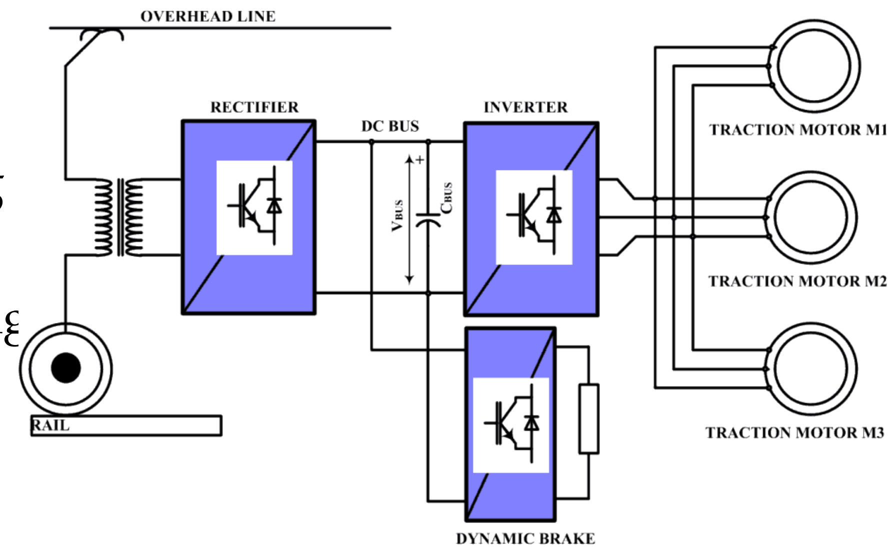
4


5


App 6: Traction

Heavy-rail Catenary Supplied Vehicles

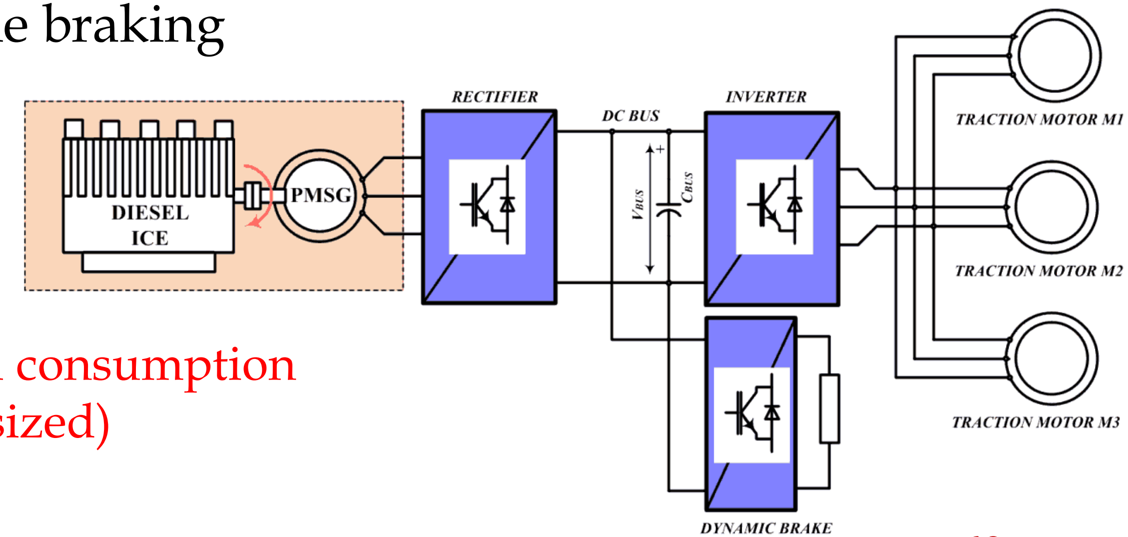
- The drive supplied from overhead line and rail via iron wheels
- Supply voltage is 25kV 50Hz and 15kV 16 2/3 Hz
    1. Step-down transformer
    2. Rectifier
    3. Traction inverters and three phase motors
    4. Dynamic brake resistor
       dc-dc converter
- Brake resistor dissipates the braking energy
    - Deceleration and down hill driving
- Braking energy is wasted
    - Low efficiency, high stress on the supply grid



App 6: Traction

Heavy-rail Diesel-supplied Vehicles

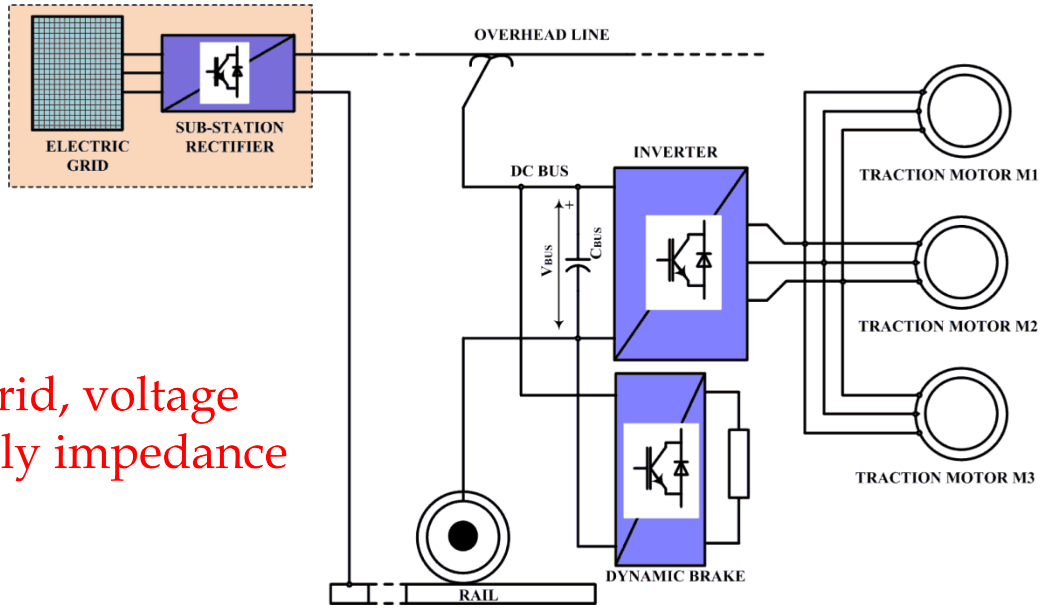
- Traditionally used in North America and in some part of Europe
    1. Diesel internal combustion engine (ICE) with three phase generator
    2. Rectifier
    3. Traction inverters and three-phase traction motors
    4. Dynamic brake resistor and dc-dc converter
- Brake resistor dissipates the braking energy
    - Deceleration, and down hill driving
- Wasted energy
    - Low efficiency, High fuel consumption and ICE stress (ICE oversized)



App 6: Traction

Light Rail Rapid Transit Vehicles

- Light rail traction drives
- Urban public transportation
- The drive is supplied from overhead line, dc voltage,1.5kV and 3kV
- On-board equipment is similar to heavy traction vehicles equipment
- The same inconveniences
- Braking energy is wasted
  - Low efficiency
  - High stress on the supply grid, voltage variations due to high supply impedance

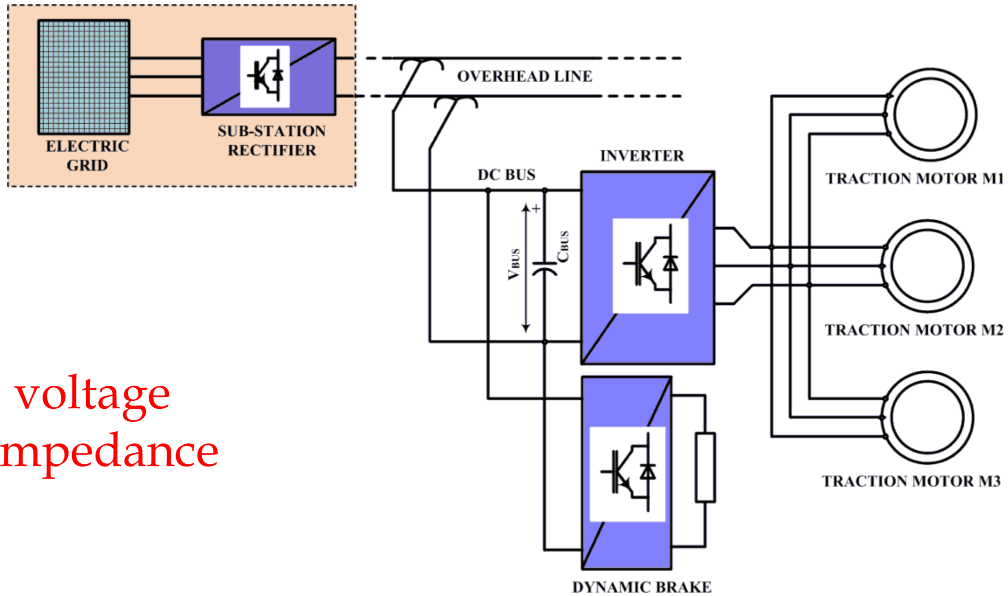


App 6: Traction

Public Transportation Catenary Supplied Vehicles

- Very similar to Light Rail Rapid Transit Vehicles
- The on-board equipment supplied from overhead lines via two pantographs
- The traction drive usually lower power rating than Public Transportation Catenary Supplied Vehicles

- The overhead dc voltage 750 V
- The same inconveniences
- Braking energy is wasted
  - Low efficiency
  - High stress on the supply grid, voltage variations due to high supply impedance



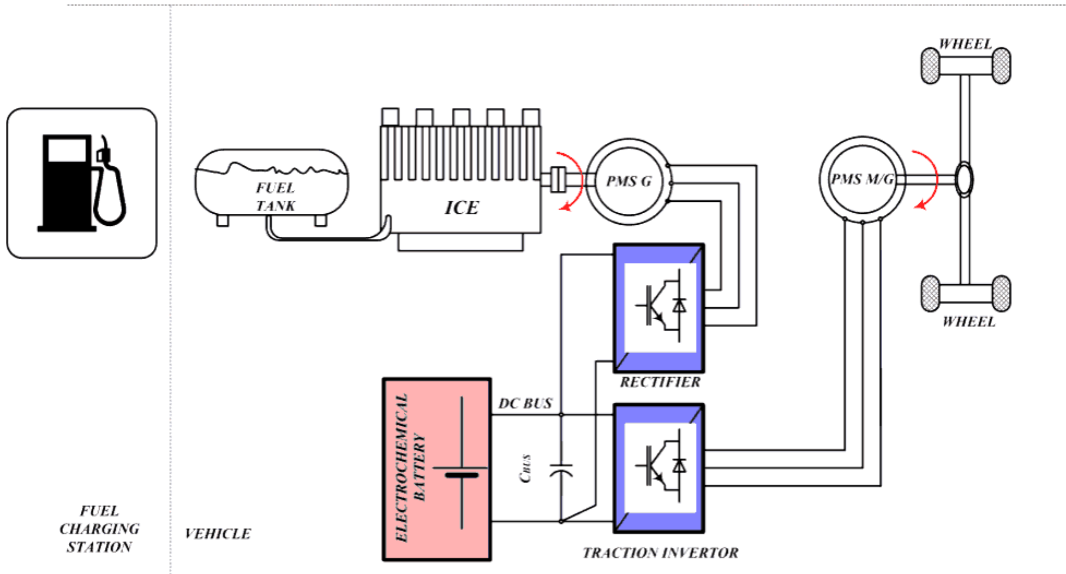
App 6: Traction

Hybrid Electric Vehicles

- Vehicles driven by a combination of an internal combustion engine (ICE) and an electric drive
- The ICE operates at the maximum efficiency point

1. ICE
2. Traction motor/generator
3. Traction inverter, and
4. Electric energy storage

- Series hybrid
- Parallel hybrid

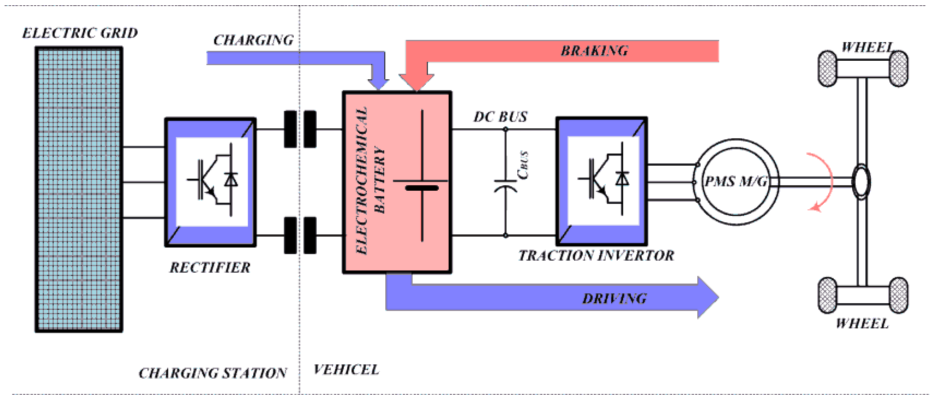


Series hybrid vehicle

App 6: Traction

Pure Electric Vehicles

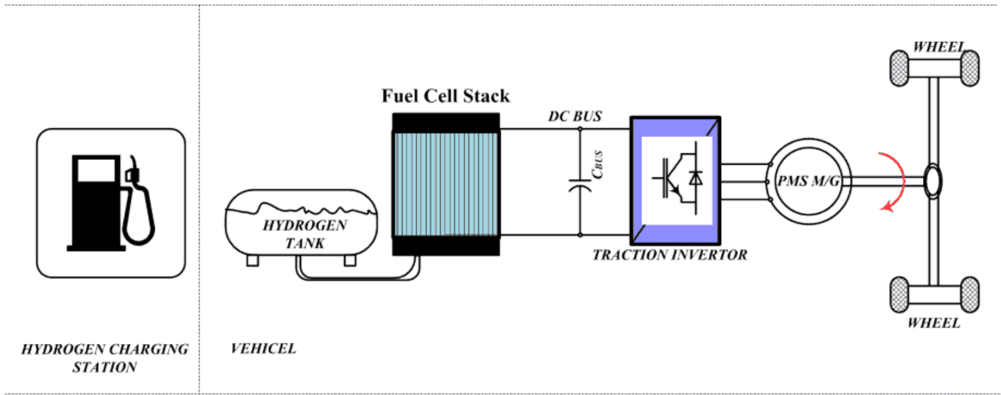
- Vehicles driven by an electric drive only
  1. Energy storage
  2. Electrochemical converter
  3. Electric traction drive



- An electrochemical converter converts stored chemical energy into electric energy

1.Electrochemical batteries
- The energy storage and electrochemical generator

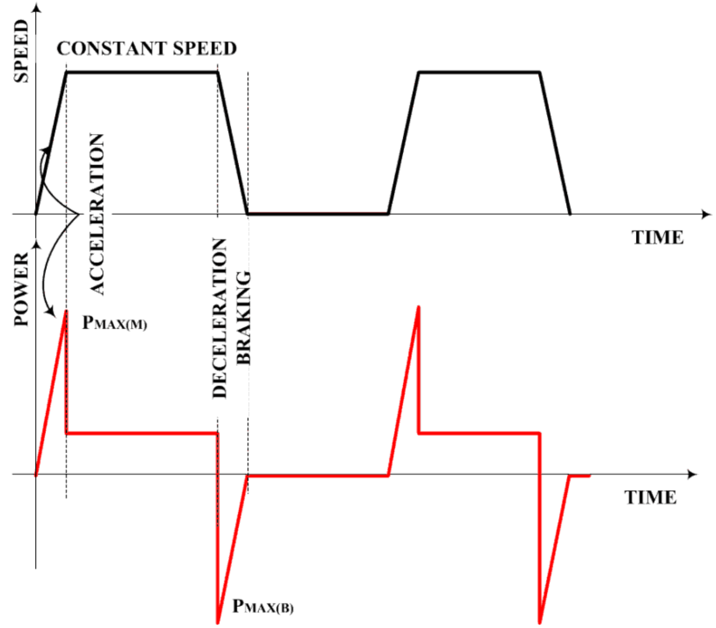
2.Hydrogen fuel cells
- Compressed hydrogen
- Fuel cell



App 6: Traction

The application issues

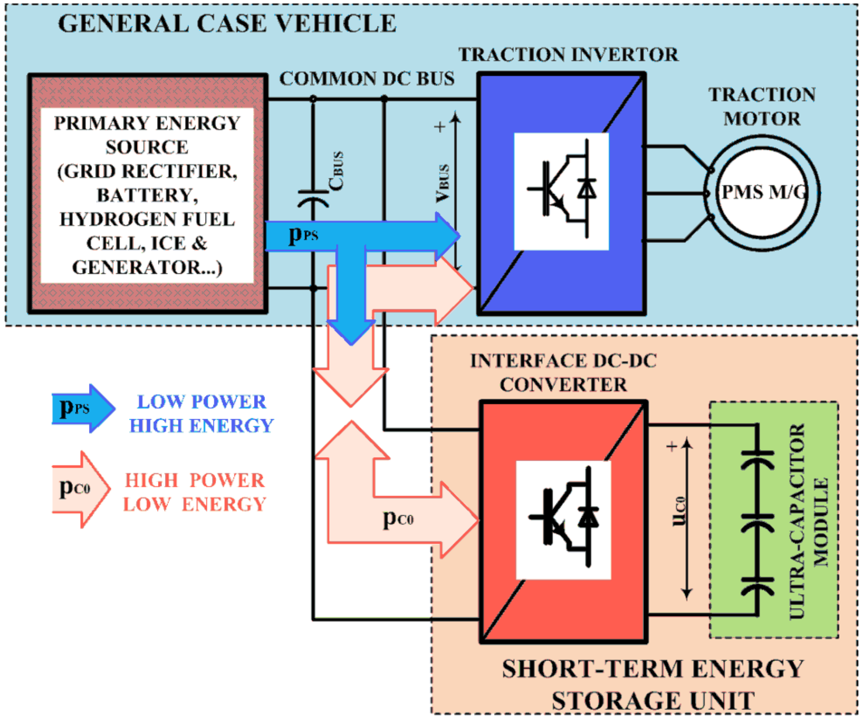
- High peak to average power ratio,
  - Highly positive power whenever the vehicle accelerates, and
  - Highly negative power whenever the vehicle decelerates
- High energy sources
  - Overhead line supply
  - Diesel ICE
  - Electrochemical batteries, fuel cells



- Sensitive on peak power
  - **Oversized**
- Do not accept negative power, partially or completely
  - **Dynamic braking resistor and mechanical brake are used**

App 6: Traction

A Common Solution

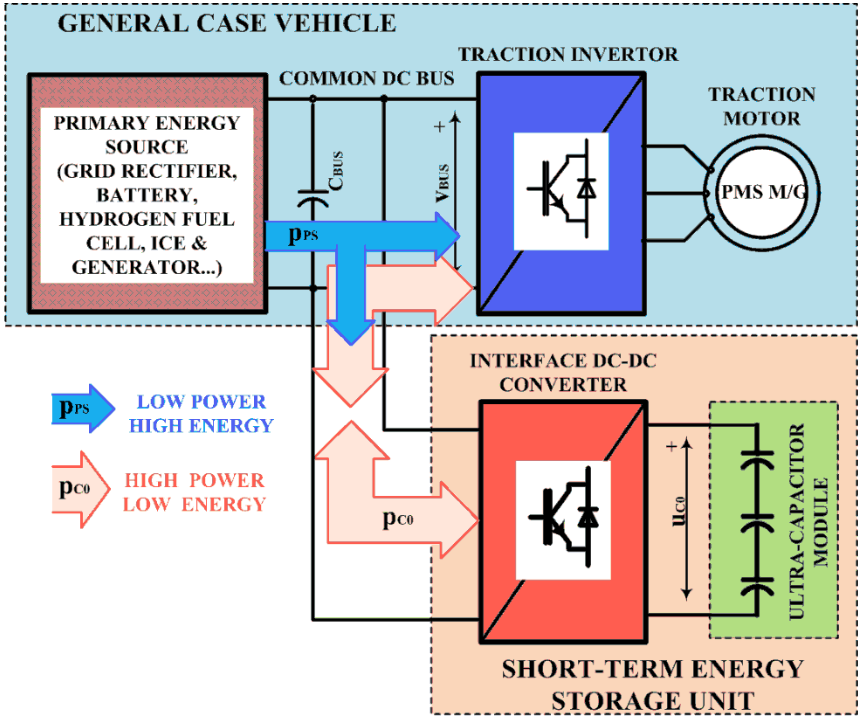


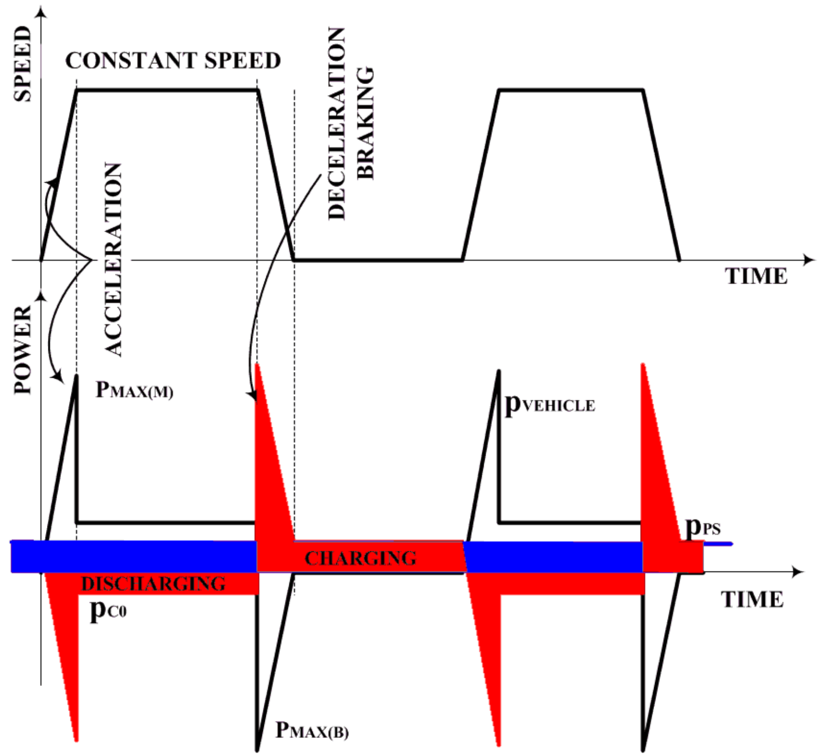
- General case vehicle
  - Common dc link
  - Voltage V_{BUS} is accessible for "the external world"
  - The vehicle is sensitive on peak power, positive as well as negative
- An external energy storage device is connected to the common dc bus
- Energy storage
  - Short term (low energy) high power energy storage device

1. An ultra-capacitor, and
2. An interface dc-dc converter

App 6: Traction

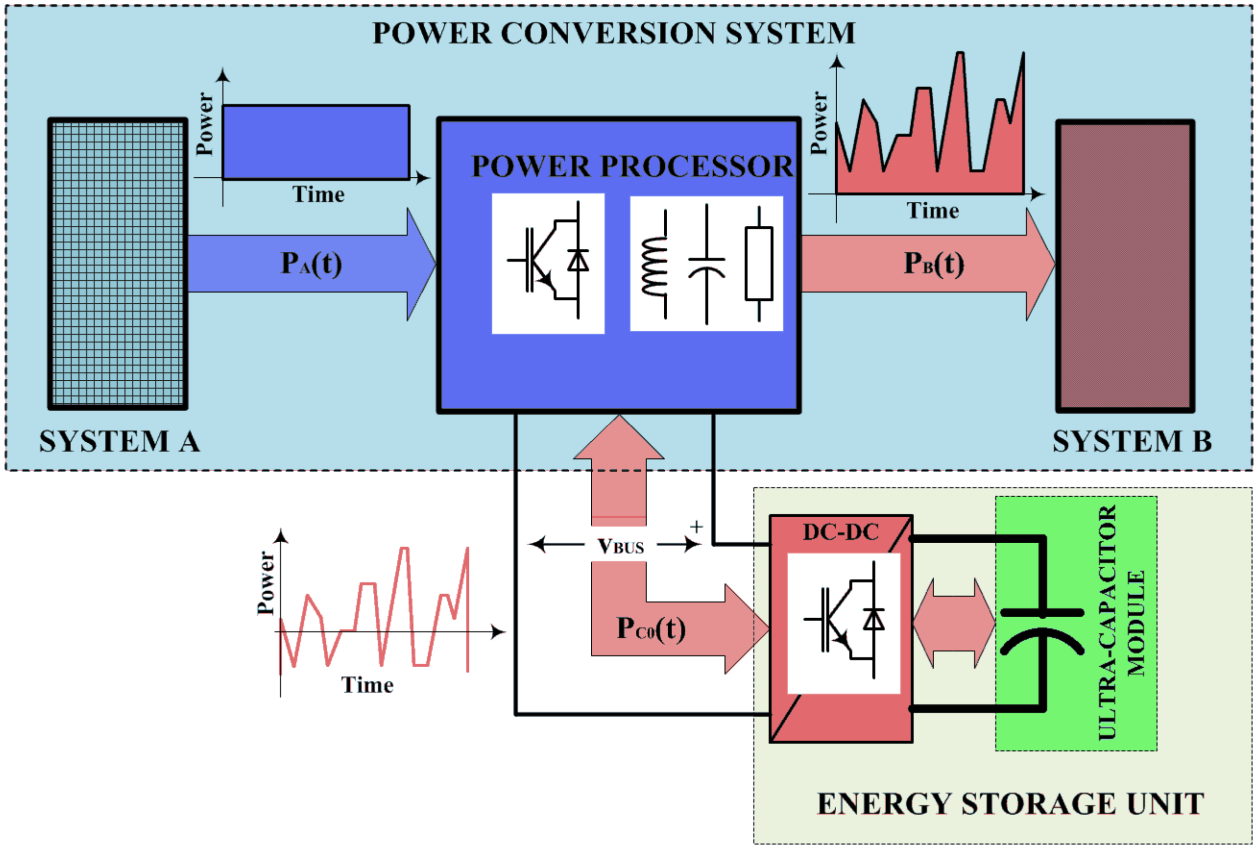
A Common Solution





The primary source power p_{PS} is smooth regardless on the traction drive load

Summary



- The same structure for all the power conversion applications:
  - Power conversion system connected with an ultra-capacitor via a dc link dc-dc convertor
- The ultra-capacitor sizing and control parameters differ from application to application

PART FOUR:
The Ultra-capacitor Selection & Design

1. Introduction
2. Voltage Rating & Capacitance
3. Losses & Conversion Efficiency
4. The Module Thermal Design
5. The Module Design-Voltage balancing
6. The Module Design Summary

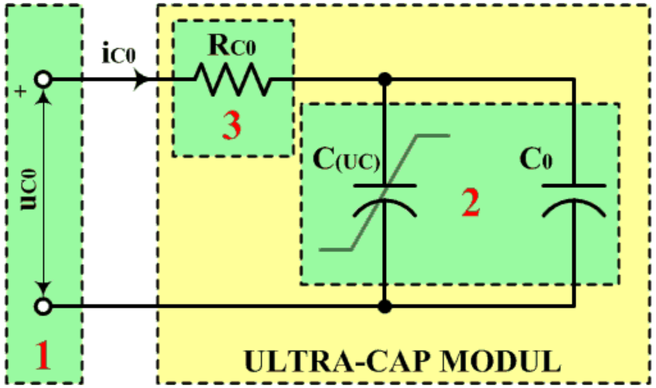
Introduction

The Objective

- Design the ultra-capacitor for the application requirements

The Fact(s)

- An ultra-capacitor is characterized by three main parameters
  1) Terminal voltage u_{C0}
     - The module voltage rating
  2) Capacitance $C_{(uc)}+C_0$
     - Energy storage capability
  3) Internal resistance R_{C0}
     - Losses, efficiency and thermal design

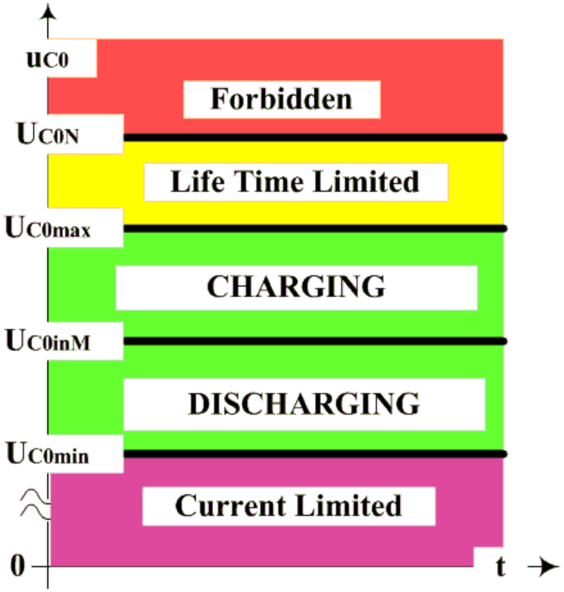


The main design steps

I. Compute the above parameters according to the application

II. Design the ultra-cap module according to the parameters

Voltage Rating & Capacitance



The parameters to be selected according to the application requirements	
1. U_{C0max}	Maximum operating voltage
2. U_{C0min}	Minimum operating voltage
3. U_{C0inM}	Intermediate operating voltage
4. U_{C0N}	The ultra-capacitor rated voltage
5. C_0	The ultra-capacitor rated capacitance
❖ R_{C0}	Equivalent series resistance
❖ C_0 and R_{C0} are not independent parameters	

Voltage Rating

1. Maximum operating voltage $\boldsymbol{U_{C0max}}$
   - depends on the dc-dc converter topology

$$U_{C0\max} \leq mV_{BUS\max}$$

$$U_{C\max} = \left[U_{C0\max}, U_{C0\max} - i_{C0}R_{C0}\right]$$

   - ***m*** is voltage gain of the interface dc-dc converter.
   - Directly connected non isolated dc-dc converter, ***m*=1**.

System	Low Voltage DC	Single Phase 110V	Single/Three Phase 230V	Three Phase 400V	Three Phase 690V
V_{BUSmax}	16 to 56V	150 to 450V	350 to 450	700 to 900V	1000 to 1200V
Application Area	Telecom, UPS, Automotive	Domestic	Domestic, Industry in Japan	Domestic and Industry	Industry

Voltage Rating

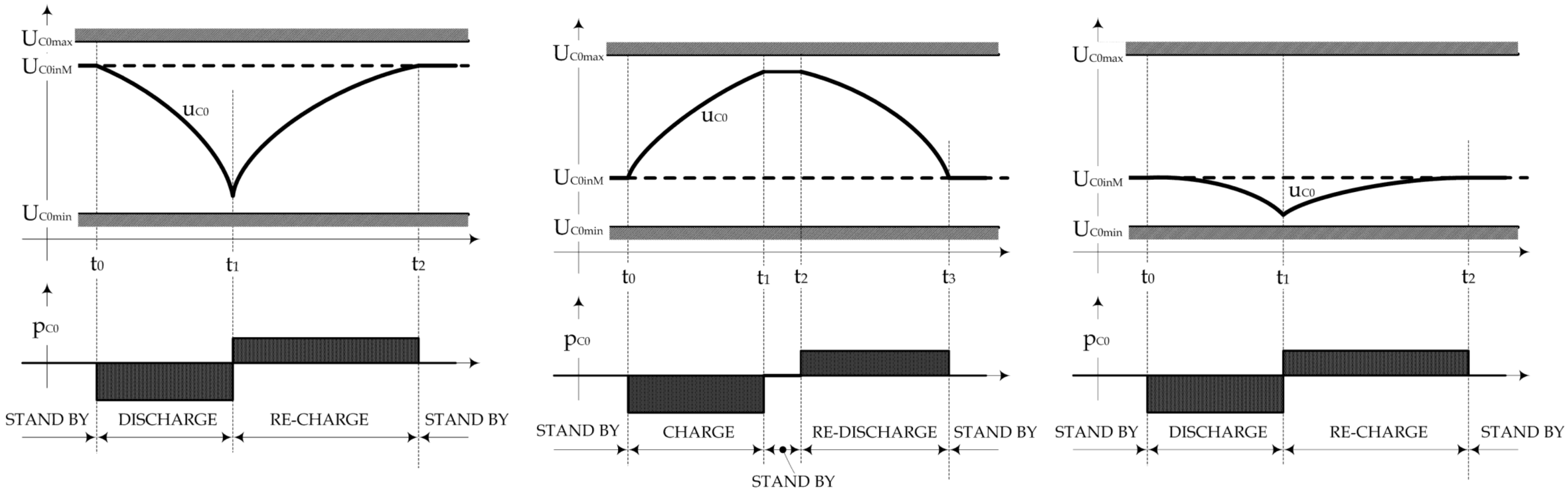
1. Minimum operating voltage $\boldsymbol{U_{C0min}}$
   - Determined by the dc-dc converter current capability assuming constant conversion power $\boldsymbol{P_{C0}}$

     $$U_{C0\min} \geq \frac{P_{C0}}{I_{C0\max}}$$

   - $U_{C\min} = \left[U_{C0\min}, U_{C0\min} + i_{C0\max} R_{C0}\right]$
   - Practically, U_{C0min} >=$0.5\ U_{C0max}$

Voltage Rating

3. Intermediate operating voltage U_{C0inM} is "a long term" average voltage. It depends on the application profile.



UPS Application

Controlled electric drive Application

Voltage Rating

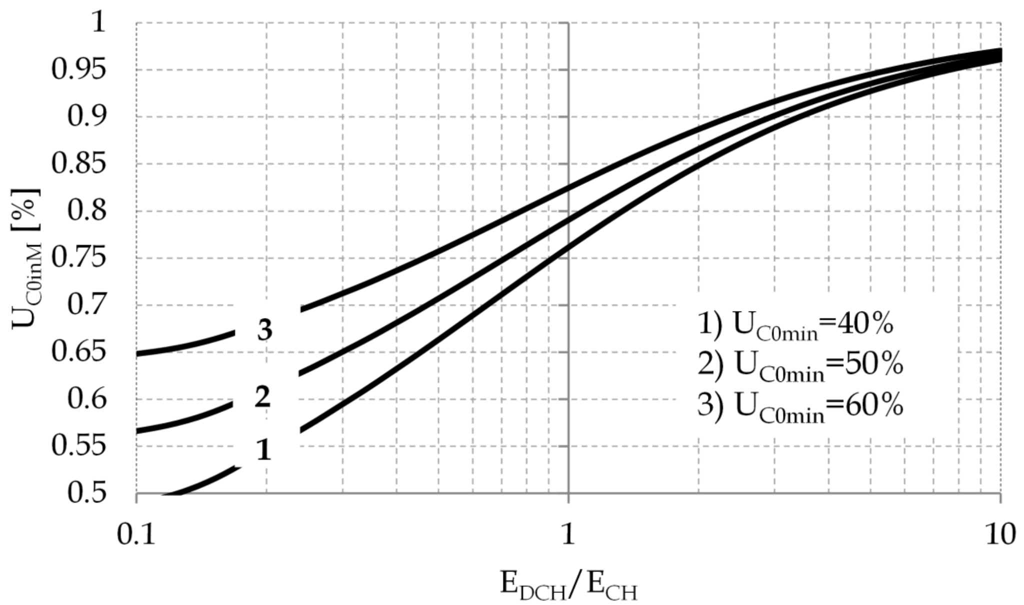
3. Intermediate operating voltage U_{C0inM}

$$U_{C0inM} \cong \sqrt{\frac{E_{DCH}U_{C0\max}^2 + E_{CH}U_{C0\min}^2}{E_{DCH} + E_{CH}}}$$

$$E_{CH} = \int_0^{T_{CH}} P_{CH}(t)dt - \int_0^{T_{CH}} R_{C0}(t) i_{C0(CH)}^2 dt$$

- Discharging energy

$$E_{DCH} = \int_0^{T_{DCH}} P_{DCH}(t)dt + \int_0^{T_{CH}} R_{C0}(t) i_{C0(DCH)}^2 dt$$



Voltage Rating

4. The ultra-capacitor rated voltage U_{C0N}
   - Determines the ultra-capacitor life time

$$T_{exp}(u_{C0},\theta) = k_1 \exp\left(\frac{u_{C0}}{U_{C0N}}k_2 + \theta k_3\right)$$

- The operating voltage u_{C0} is not constant
- Average life time for a given voltage profile $u_{C0}(t)$ and temperature profile $\theta(t)$

$$T_{AV}(U_{C0N},\theta) = \psi(u_{C0}(t),\theta(t))$$

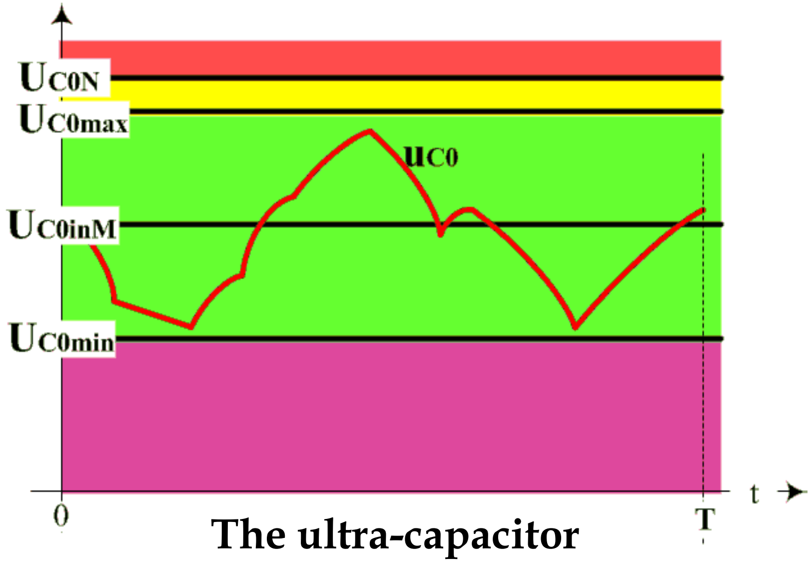
- Voltage rating U_{C0N} for expected life time

$$U_{C0N} = f(T_{AV},\theta)$$

θ The ultra-capacitor operating temperature

u_{C0} The ultra-capacitor operating voltage

k_1, k_2, k_3 Coefficients



The ultra-capacitor voltage profile

Capacitance

5. The ultra-capacitor rated capacitance
   - Voltage dependent capacitor

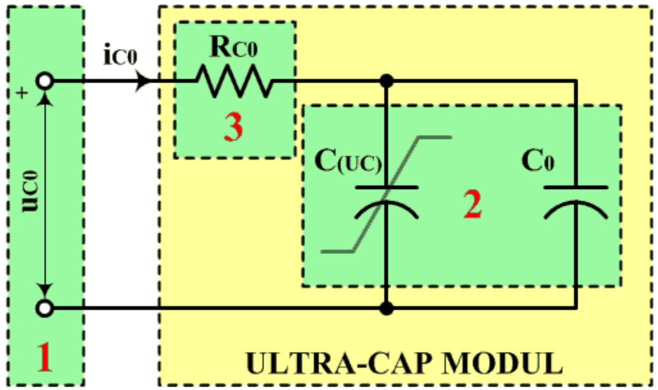
$$C(u_C) = C_0 + C(u_C) = C_0 + k_C \cdot u_C$$

   - The initial capacitance C_0

$$C_0 = \left(E_{CH} - \frac{2}{3}k_C\left(U^3_{C0\max} - U^3_{C0inM}\right)\right)\frac{2}{\left(U^2_{C0\max} - U^2_{C0inM}\right)}$$

     - U_{C0max}, U_{C0max} and E_{CH}, from (4.1),(4.3) and (4.4).
   - The ultra-capacitor approximated as a linear capacitor (***kc*=*0***)

$$C_0 \cong \frac{2E_{CH}}{\left(U^2_{C0\max} - U^2_{C0inM}\right)}$$



   - The capacitance is (4.11) determined for the energy capability (4.4)
   - Is there another criterion to define the capacitance?
     - Conversion efficiency, cost, or something else?

Losses & Conversion Efficiency

- The ultra-capacitor losses

$$P_C(t) \cong R_{C0} P_{C0}^2 \begin{cases} \dfrac{C_0}{C_0 U_{C0\min}^2 + 2P_{C0}t} & \text{CHARGING} \\ \dfrac{C_0}{C_0 U_{C0}^2 - 2P_{C0}t} & \text{DISCHARGING} \end{cases}$$

- Valid only and only if the ultra-capacitor internal resistance is constant at the frequency of interest
- If not a case, the losses must be computed as frequency dependent losses

$$P_{AV}(T) = \frac{1}{2} \sum_{k=0}^{+\infty} R_{C0}(k\omega_0) \cdot I_{0(k)}^2$$

Losses & Conversion Efficiency

- The energy dissipated during one charge cycle

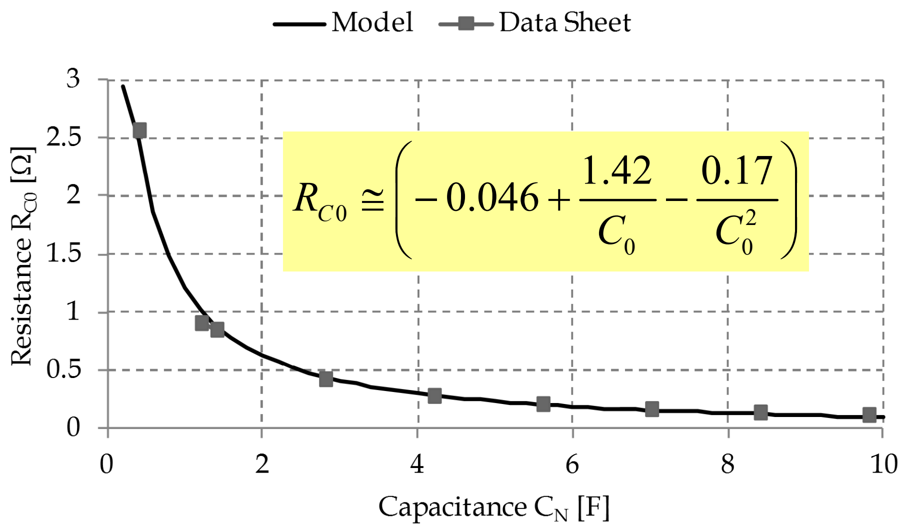
$$E_{LOSSES} \cong R_{C0} P_{C0}^2 \int_0^{T_{CH}} \frac{C_0}{C_0 U_{C0\max}^2 - 2E_{CH} + 2P_{C0} t} dt = \frac{R_{C0} P_{C0} C_0}{2} \ln \frac{C_0 U_{C0\max}^2}{C_0 U_{C0\max}^2 - 2E_{CH}}$$

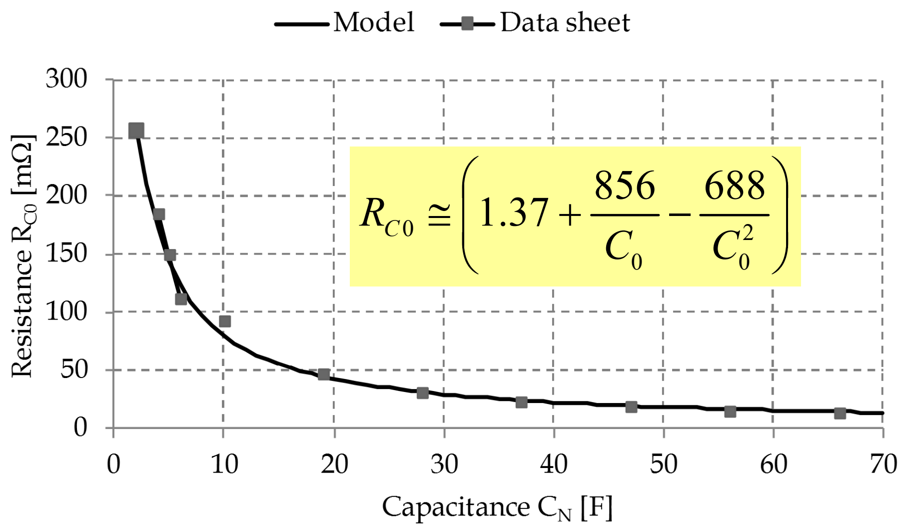
  - The resistance $\boldsymbol{R_{C0}}$ depends on the capacitance $\boldsymbol{C_0}$

$$\frac{\partial R_{C0}}{\partial C_0} = \frac{\partial \left[R_{C0}(C_0) \right]}{\partial C_0} < 0$$

$$R_{C0} = \left(k_{RC(0)} + \frac{k_{RC(1)}}{C_0} + \frac{k_{RC(2)}}{C_0^2} \right)$$

Losses & Conversion Efficiency



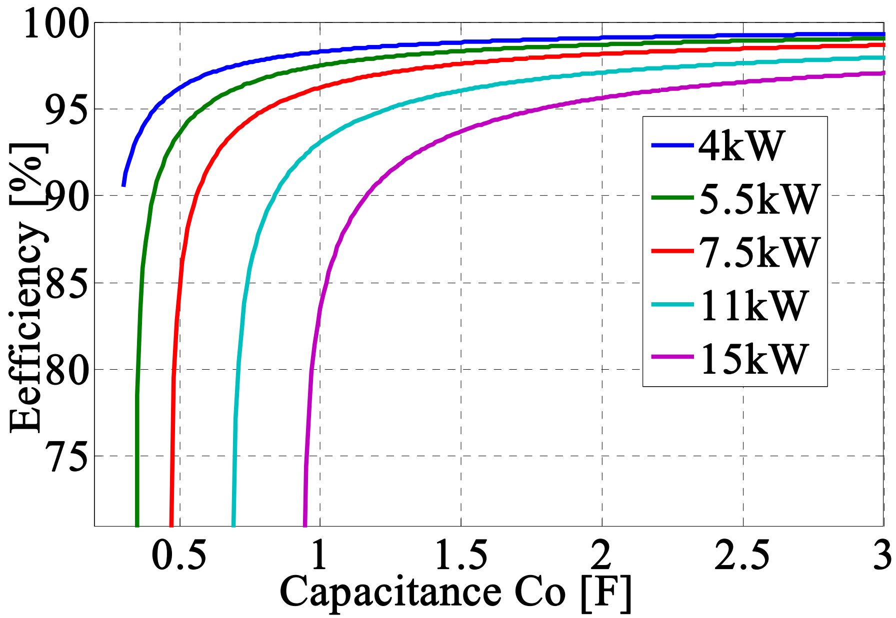


The ultra-capacitor module resistance versus capacitance. The module rated voltage U_{C0N}=800V

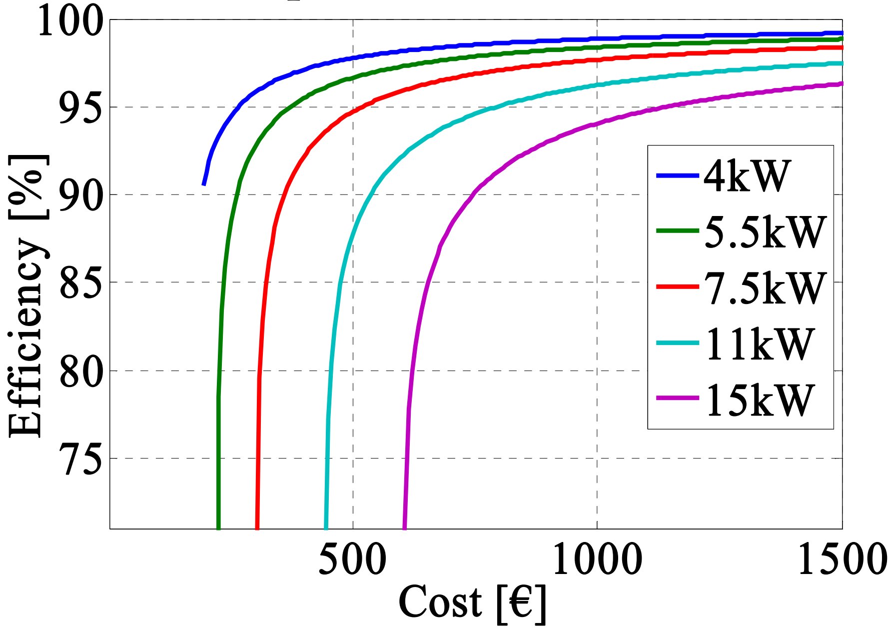
Losses & Conversion Efficiency

- Round trip efficiency is a function of the capacitance C_0

$$\eta = 100\left(1 - 2\frac{E_{LOSSES}}{E_{CH}}\right) = \eta(C_0)$$



- Round trip efficiency is a function of the capacitor cost



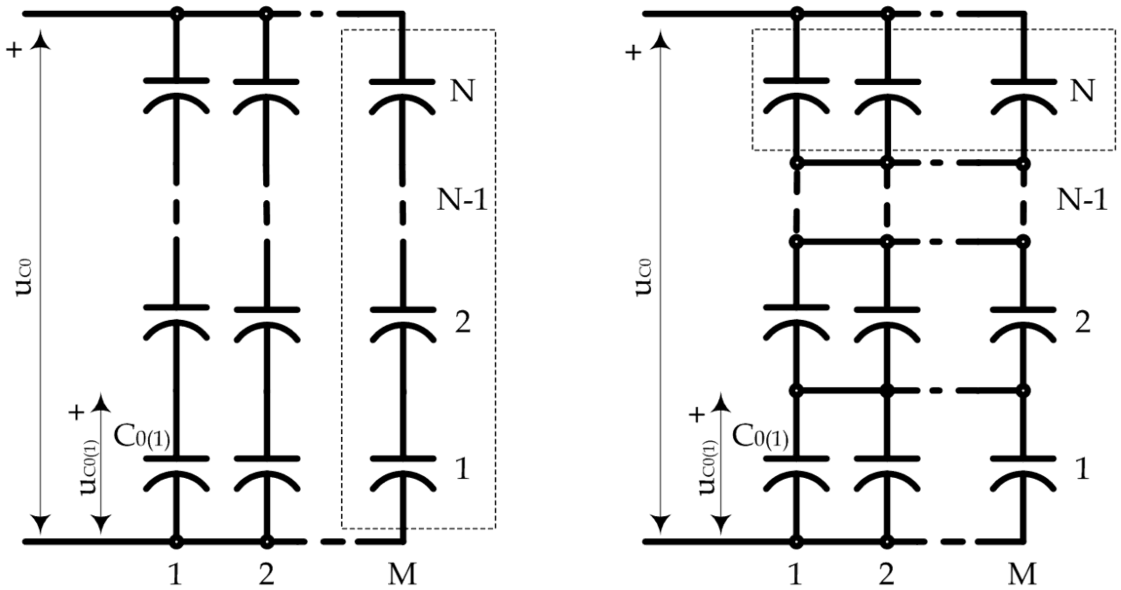
The Module Design

- Series-parallel Connection
- N number of series connected cells

$$N = floor\left(\frac{U_{C0N}}{U_{CON(cell)}}\right)$$

- M number of parallel connected cells

$$M = floor\left(\frac{C_N}{C_{N(cell)}}\right)N$$

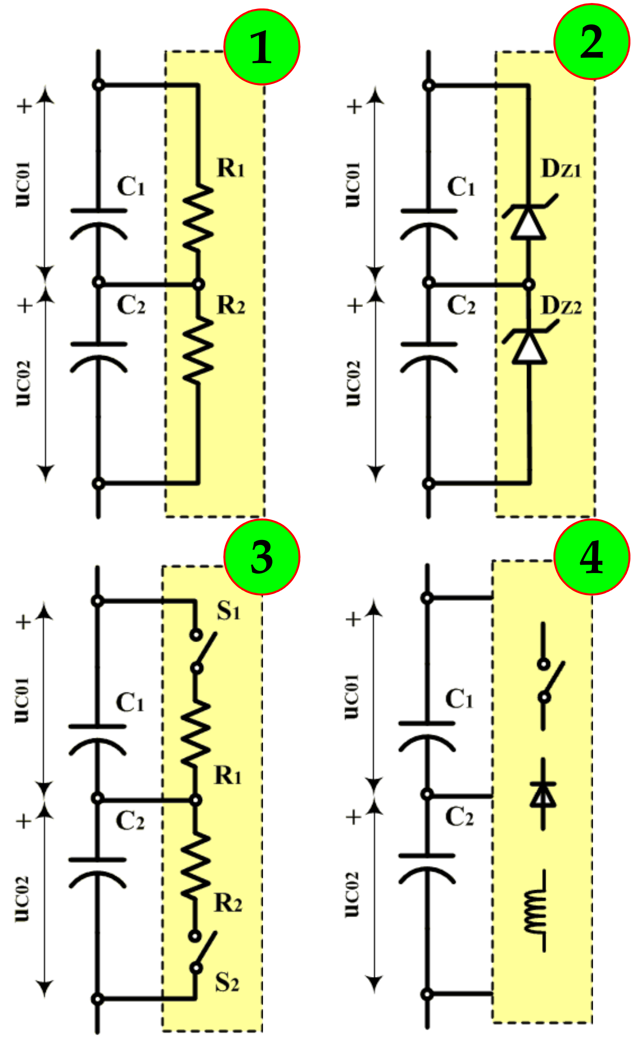


Voltage Balancing

- An elementary cell voltage is low U_{C01}~2.7V,
  - Not sufficient for power conversion applications
    - U_{C0N} is tens and hundreds volts
    - Tens and hundreds of cells series connected
- Total module voltage may not be equally distributed
  1. Dispersion of the cells capacitance, ~ +/- 20%
     - Dynamic variation of the voltage $\frac{1}{C_{01}}\int i_{C0}dt \neq \frac{1}{C_{02}}\int i_{C0}dt ...... \neq \frac{1}{C_{0n}}\int i_{C0}dt$
  2. Dispersion of the cells equivalent series resistance
     - Dynamic variation of the voltage $R_{C01}i_{C0} \neq R_{C02}i_{C0} .... \neq R_{C0n}i_{C0}$
  3. Dispersion of the cells leakage current $\frac{1}{C_{01}}\int i_{01}dt \neq \frac{1}{C_{02}}\int i_{02}dt ...... \neq \frac{1}{C_{0n}}\int i_{0n}dt$
     - Long term voltage variation
- A voltage balancing circuit is required to prevent the cell overvoltage and the life time degradation

Cell Voltage Balancing

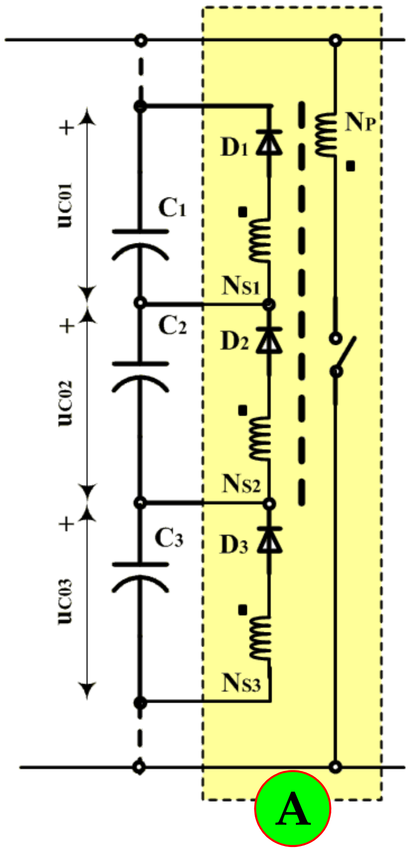
1. Passive resistive balancing circuit
   - Additional leakage current , low efficiency, high reliability, no dynamic balancing capability
2. Passive voltage clamping circuit
   - The cell voltage is limited but not equally distributed on the cells, limited dynamic balancing capability
3. Switched resistor balancing circuit
   - Voltage actively controlled, low efficiency, limited dynamic balancing capability
4. Switch mode balancing circuit
   - Voltage actively controlled, good balancing capability, high efficiency, high complexity



Cell Voltage Balancing

- Switch mode balancing circuit,
  - Active voltage sharing control,
  - Good balancing capability,
  - High efficiency,
  - High complexity

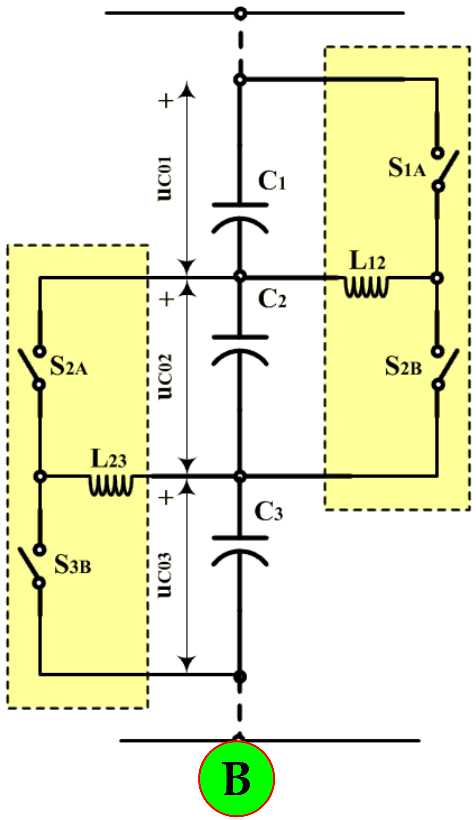
A. Centralized fly-back converter
  - No feedback control is required,
  - Multi-winding transformer is complex



Cell Voltage Balancing

- Switch mode balancing circuit,
  - Active voltage sharing control,
  - Good balancing capability,
  - High efficiency,
  - High complexity

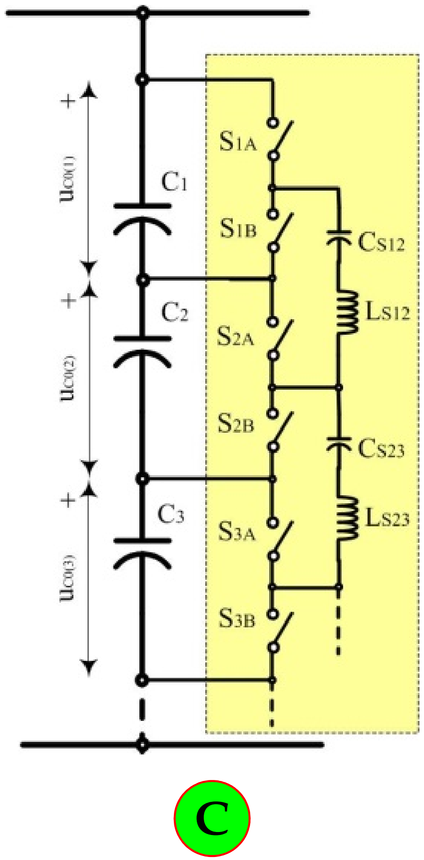
B. Decentralized half bridge
  - Simple inductors ***n*-1**
  - Feedback control is required,
  - High number of switches **2*n*-2**
  - Complex control and driving circuit
  - Over-voltage and Si power



Cell Voltage Balancing

- Switch mode balancing circuit,
  - Active voltage sharing control,
  - Good balancing capability,
  - High efficiency,
  - High complexity

C. Resonant Decentralized half bridge
  - Simple LC resonant circuit ***n-1***
  - Feedback is not required,
  - No overvoltage
  - High number of switches ***2n***
  - Complex driving circuit and resonance tracking



The Module Design Summary

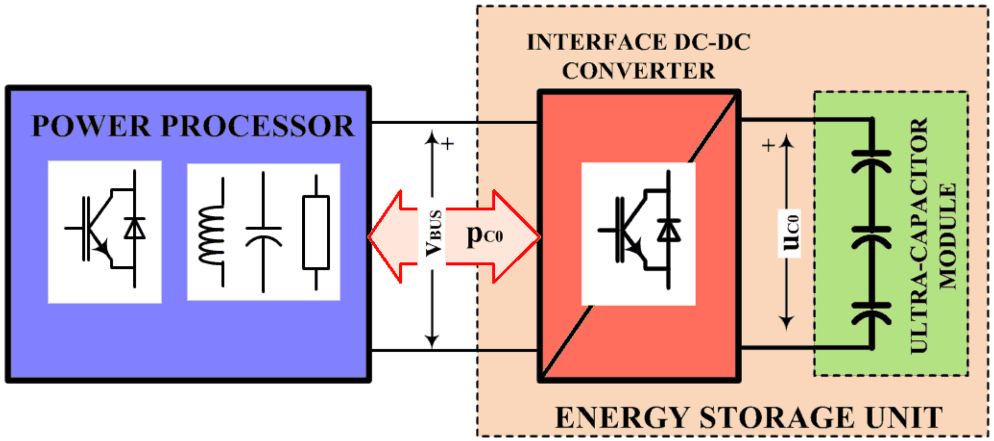
Step 1	Select the module rated voltage	$U_{C0N} = f(T_{AV}, \theta)$
Step 2	Select the module capacitance for given energy capability or efficiency required	$C_0 \cong \frac{2E_{CH}}{\left(U^2_{C0\max} - U^2_{C0inM}\right)}$ $\eta = \eta(C_0)$
Step 3	Number of series connected sub-cells	$N = \mathrm{int}\left(\frac{U_{C0N}}{U_{C0N1}}\right)$
Step 4	Capacitance of a sub-cell	$C_{01} > C_0 N$
Step 5	Number of parallel connected cells	$M = \mathrm{int}\left(\frac{C_{01}}{C_{0C}}\right)$
Step 6	Thermal design	If needed, go to step 4, select new cell and repeat steps 5 and 6
Step 7	Voltage balancing circuit	

PART FIVE:
The Interface Converter

1. Introduction
2. State of the Art
3. The Converter Design
4. Design Example
5. Control of The Interface Converter
6. Controller Design Example

Introduction

- Flexible and controllable interface between the ultra-capacitor and the power processor
  - Required due to **the ultra-capacitor and battery** voltage to SOC characteristic
  - For the system flexibility, controllability and efficiency
  - The interface is a bidirectional **dc-dc or dc-ac** power convertor
  - The dc-dc converter control
  - To control of the dc bus voltage V_{BUS}, the ultra-capacitor SOC (u_{C0})…etc.
  - The control can be independent from the power processor control



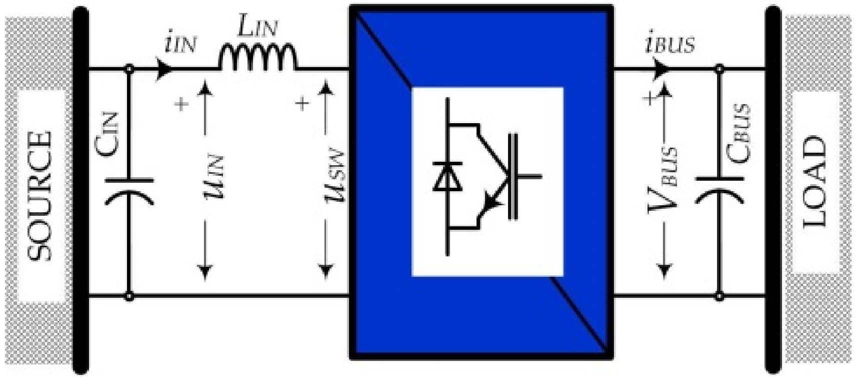
Voltage or Current Source

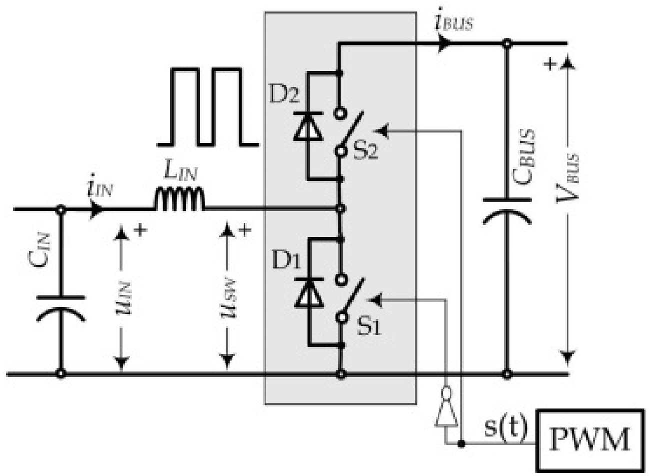
Current Source Converters

-Switch the current instead of voltage-

...Current Source Converters ...

- Theory of Duality
  - Voltage ↔ Current, Inductor ↔ Capacitor, Node ↔ loop, Series ↔ parallel
- PWM Voltage Source ↔ Current Source Converter

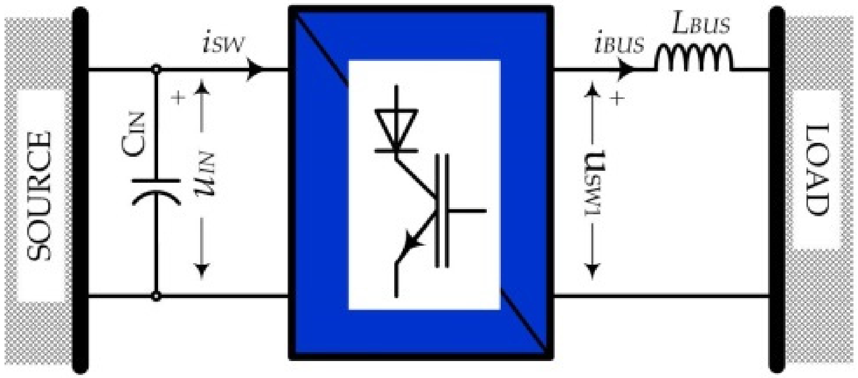


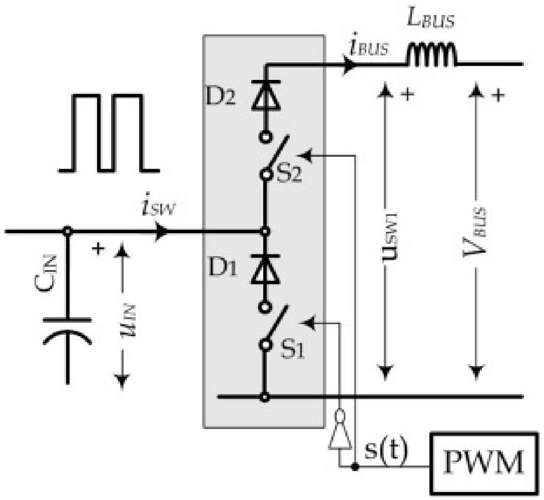


Voltage Source Converter VSC

...Current Source Converters ...

- Theory of Duality
  - Voltage ↔ Current, Inductor ↔ Capacitor, Node ↔ loop, Series ↔ parallel
- PWM Voltage Source ↔ Current Source Converter

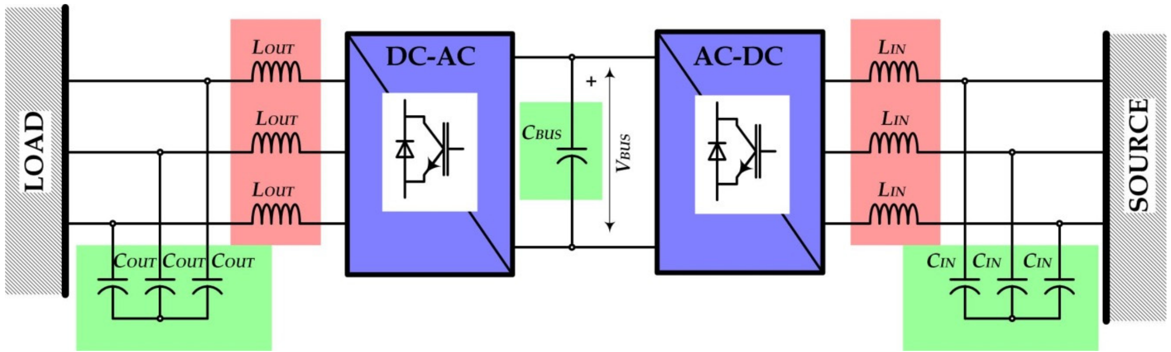




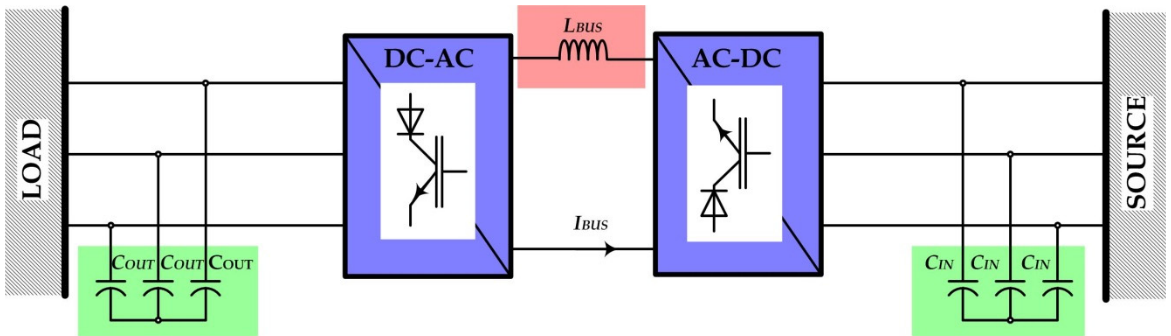
Current Source Converter CSC

...Current Source Converters ...

- 3 Phase PWM VSC
  - 1 dc bus capacitor
  - 6 big filter Inductors
  - 6 Filter capacitors



- 3 Phase PWM CSC
  - 1 dc bus Inductor
  - 6 big filter Caps.

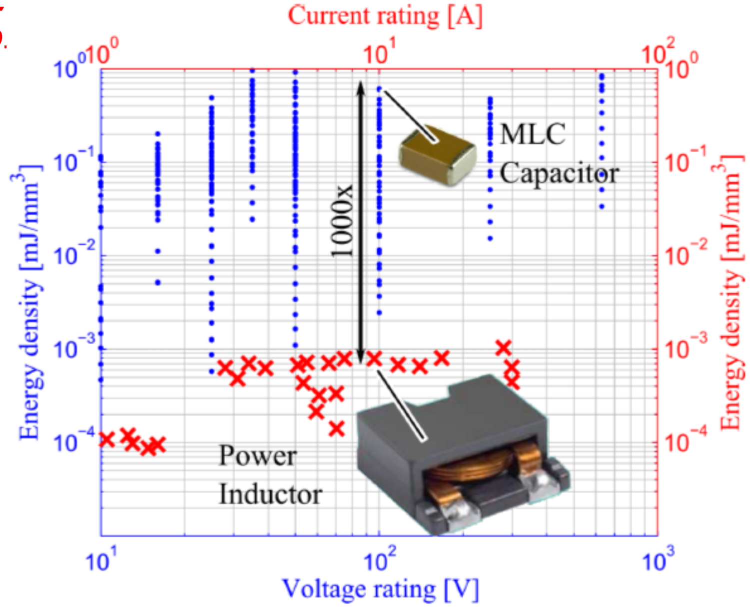


- Is there any difference between VSC & CSC?

...Current Source Converters ...

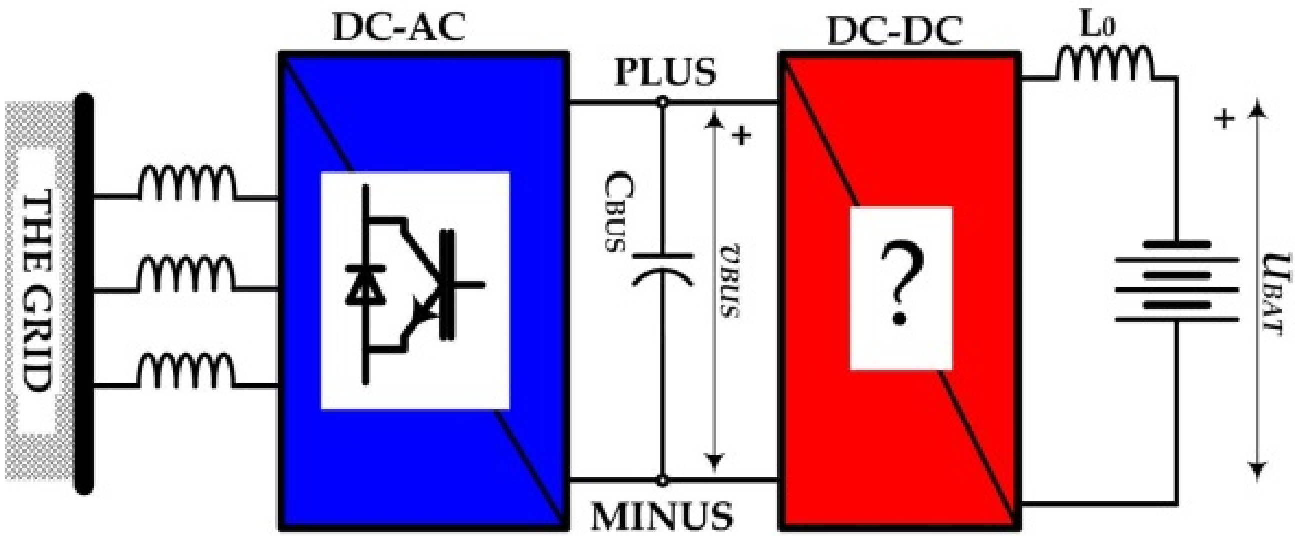
- Is there any difference between VSC & CSC?
- Energy Density of Capacitors and Inductors
  - Film Caps. W_C=40-80 [J/kg]
  - **MLCC much better**
  - MF Inductors W_L=0.2-1 [J/kg

The CSC should be better than the VSC?

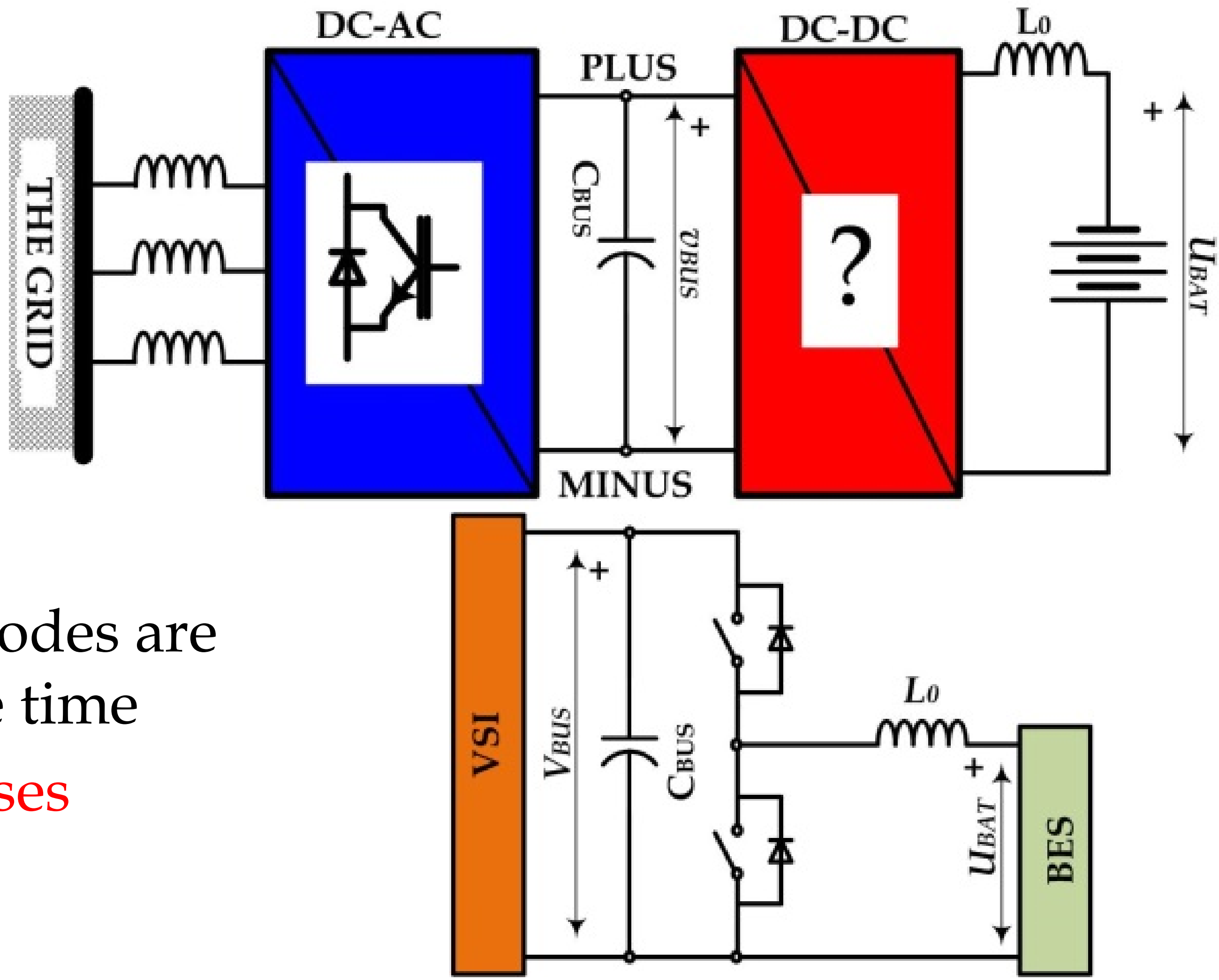


Robert Pilawa-Podgurski, "High density capacitor-based power converters - application challenges and requirements" March 3rd, 2018PSMA/PELS Capacitor Workshop

...Current Source Converters ...



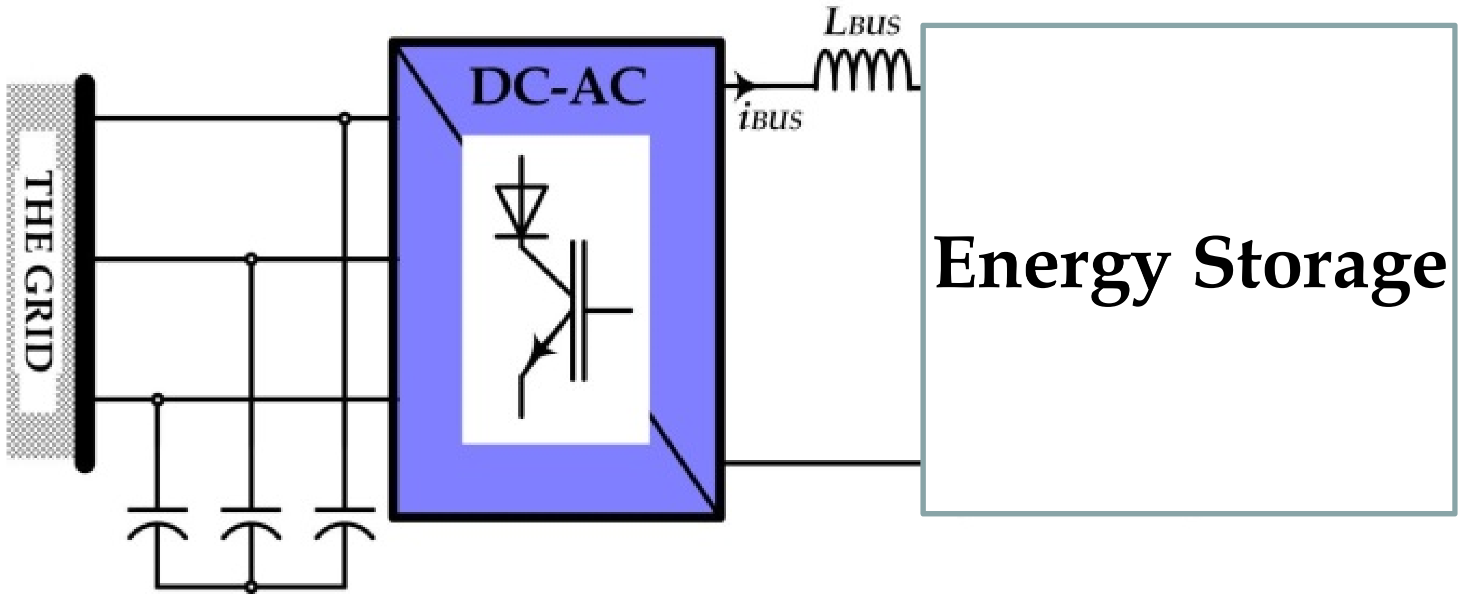
...Current Source Converters ...



Switches and Diodes are switching all the time

- Switching losses
- Inductor L_0

...Current Source Converters ...



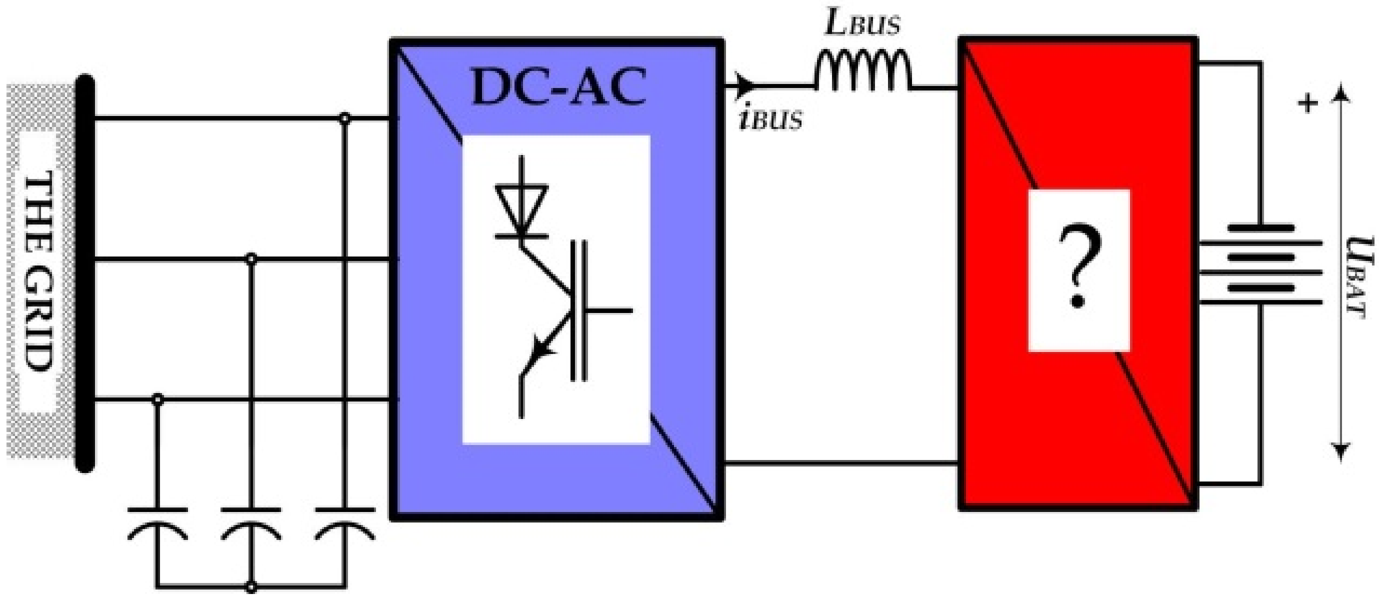
CSC

- Current i_{BUS} positive and only positive
- Voltage V_{BUS} positive or negative

Energy Storage

- Current positive or negative
- Voltage positive and only positive

...Current Source Converters ...



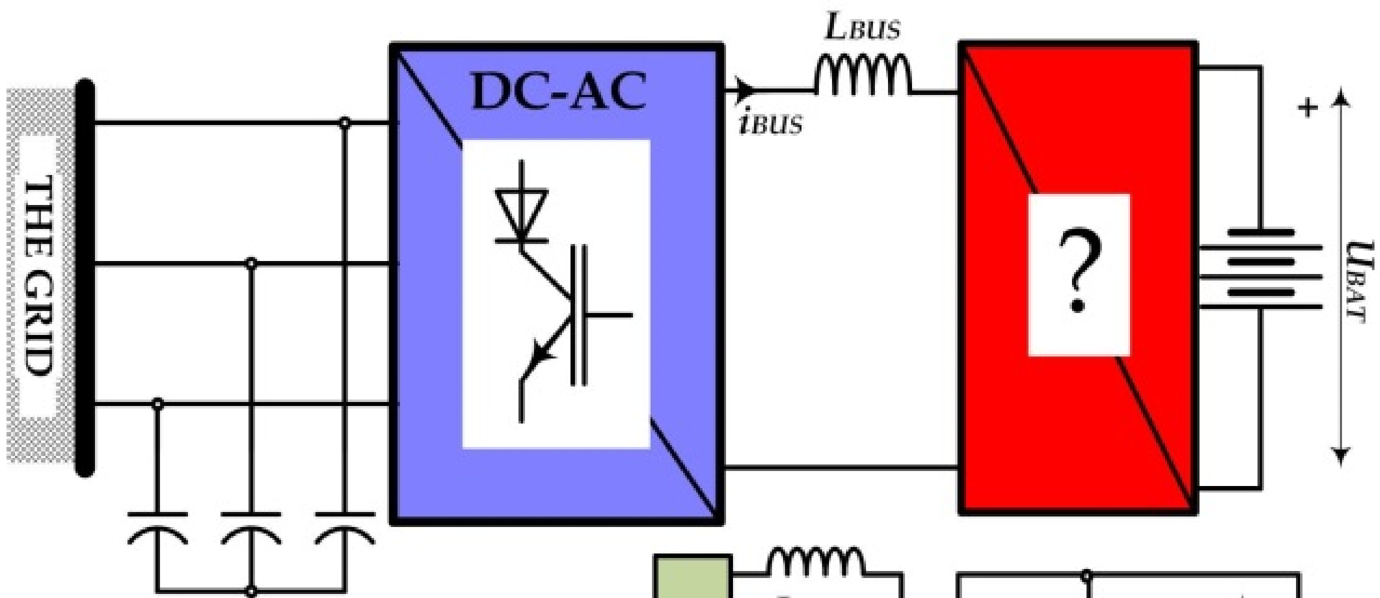
CSC

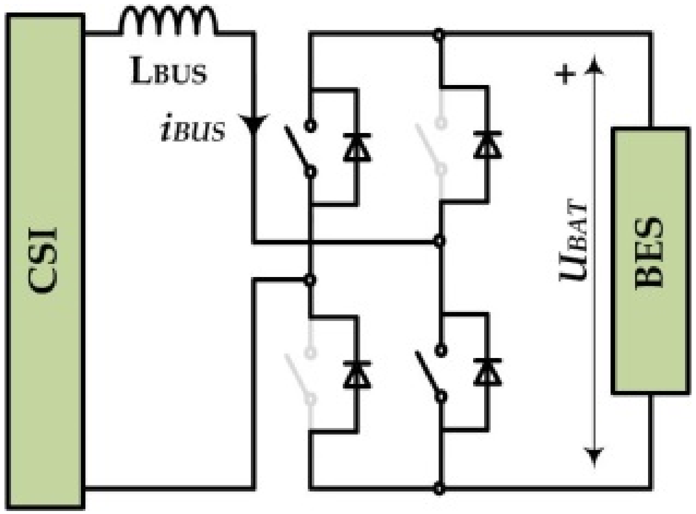
- Current i_{BUS} positive and only positive
- Voltage V_{BUS} positive or negative

Energy Storage

- Current positive or negative
- Voltage positive and only positive

...Current Source Converters ...





Charging

Diodes conducting

Discharging

Switches conducting

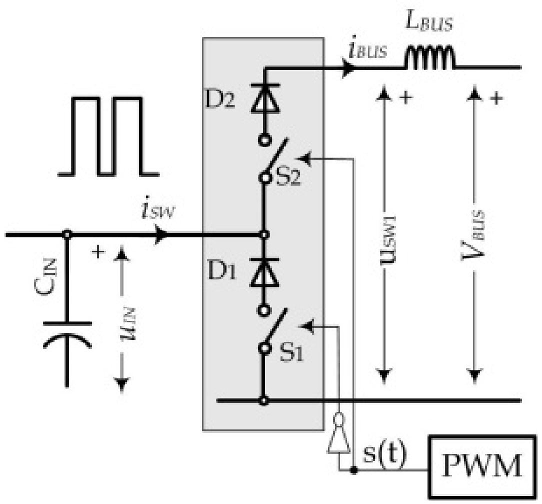
No switching losses!

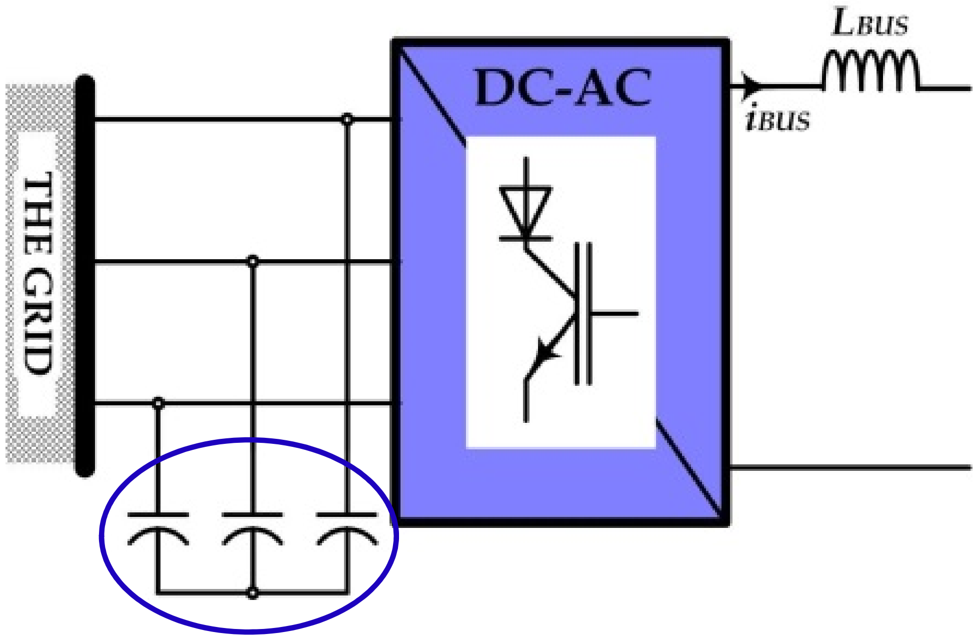
...Current Source Converters ...

- It looks like CS Converters have bright future?

...Current Source Converters ...

- It looks like CS Converters have bright future?
  - Yes But, “No meal for free”



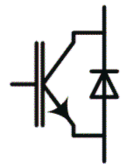


Grid Filter caps C_{IN} are stressed with high current pulses !!

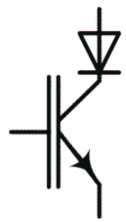
⇒ Relatively big caps….⇒ The Grid is not very happy !!

...Current Source Converters ...

- It looks like CS Converters have bright future?
  - Yes But, “No meal for free”
- Existing power semiconductors are perfectly matched with PWM VSCs
  - Current bi-directional Switch…MOSFETs, IGBTs+FWD….



- PWM CSCs require different switch
  - Voltage Bi-directional Switch, but high frequency

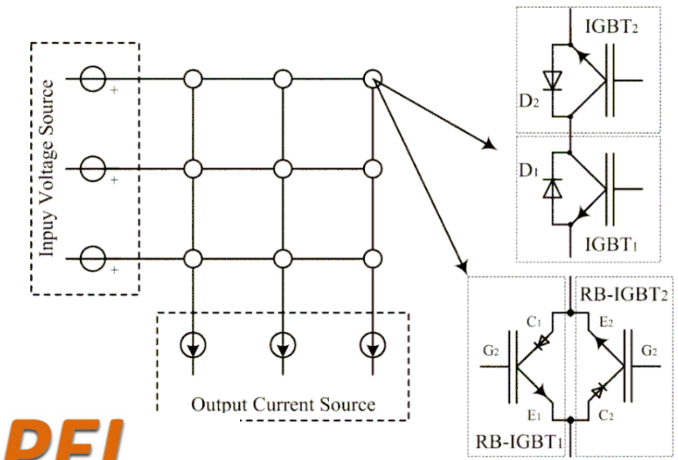


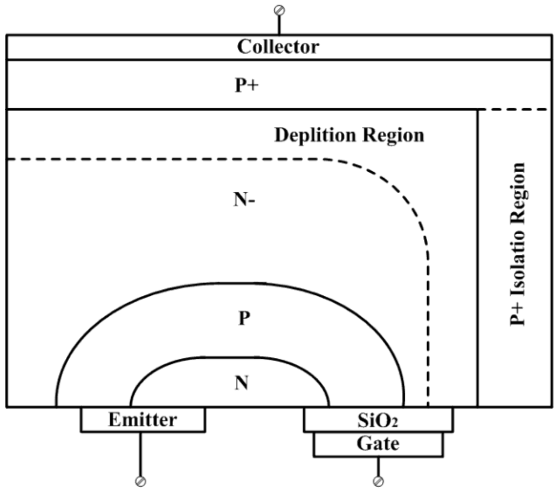
- This should be focus for future research

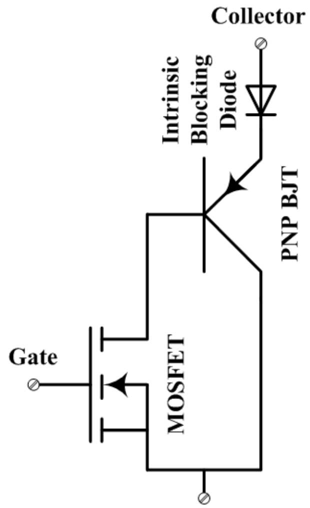
...Current Source Converters ...

Reverse Blocking IGBT

- An IGBT is naturally reverse blocking device, but....
- Not required in most of applications
  - Minimized to optimize the switching performances
  - Typically 10-50V
- Matrix and current source converters requires full RB capability
- Additional p+ layer provides full RB capability
  - An "intrinsic" blocking diode
- Better conduction performances, but worst switching (turn-off)
  - Preferred solution in low frequency range <10kHz
- The same dynamic modal as an ordinary IGBT







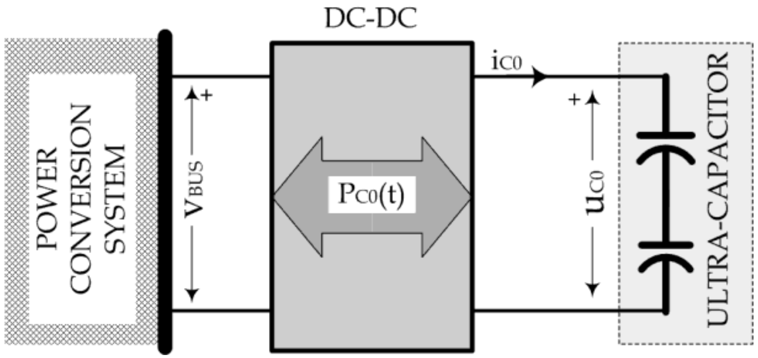
Full Power or Partial Power Converters

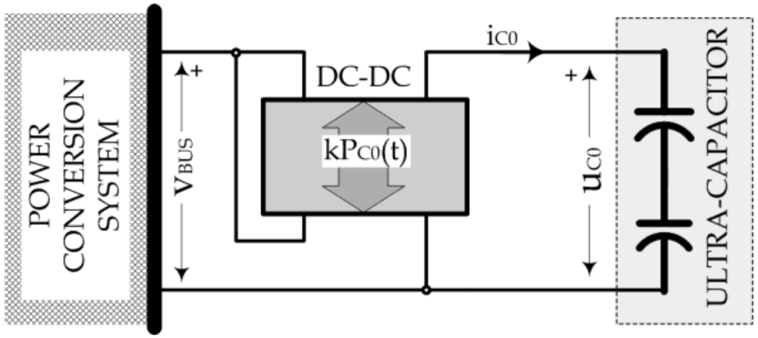
C. Full power rated converter

$$P_{DC-DC} = P_{C0}$$

D. Partial power rated converter

$$P_{DC-DC} = P_{C0}\left(1 - \frac{U_{C0\,min}}{V_{BUS}}\right) < P_{C0}$$

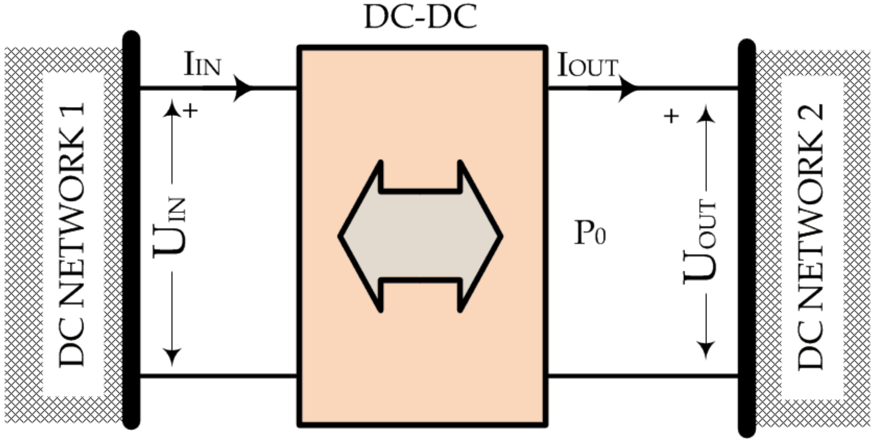


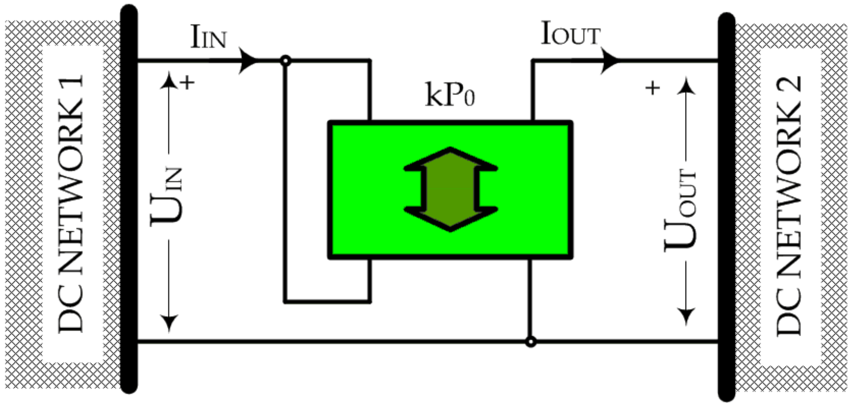


Partial Power Rated Converters

-Process a Fraction of Power-

...Partial Power Rated Converters...





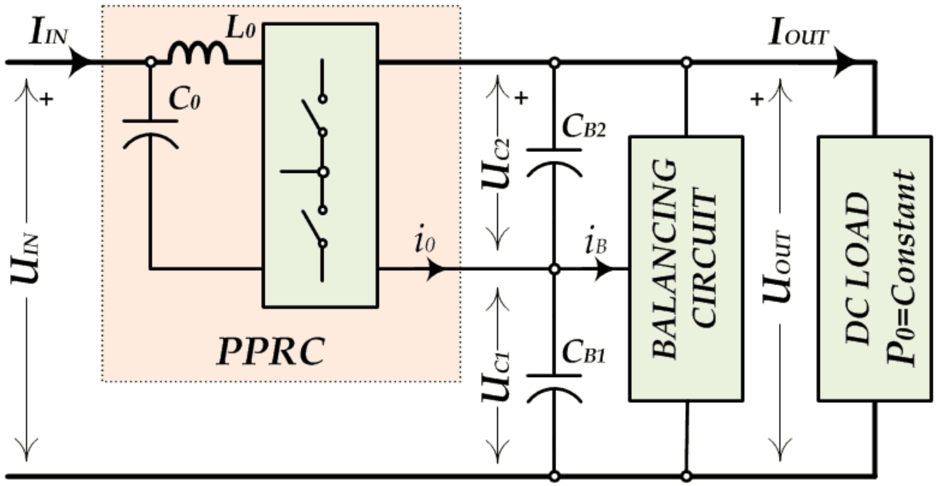
Full Power Rated Converter

- ❑ The converter is handling total power
- ❑ Size, Cost, Efficiency

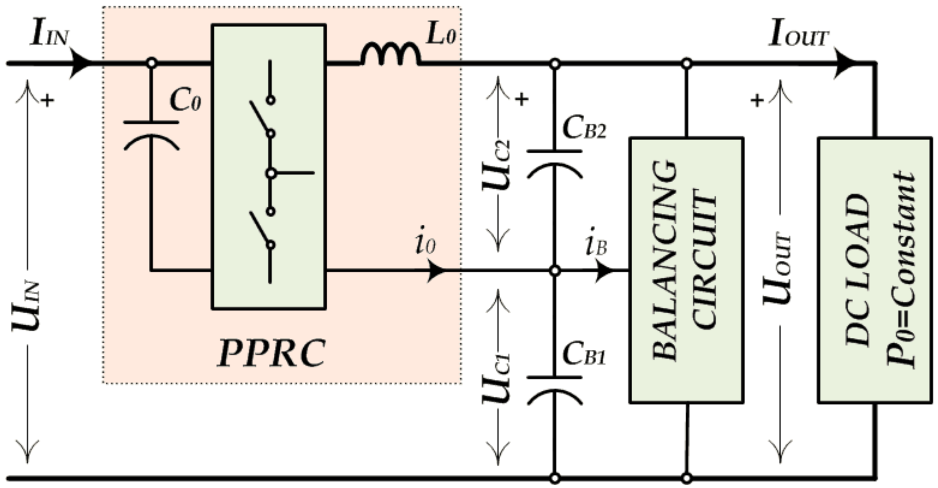
Partial Power Rated Converter

- ❑ The converter is handling just a fraction of total power
- ❑ Size, Cost, Efficiency

...Partial Power Rated Converters...

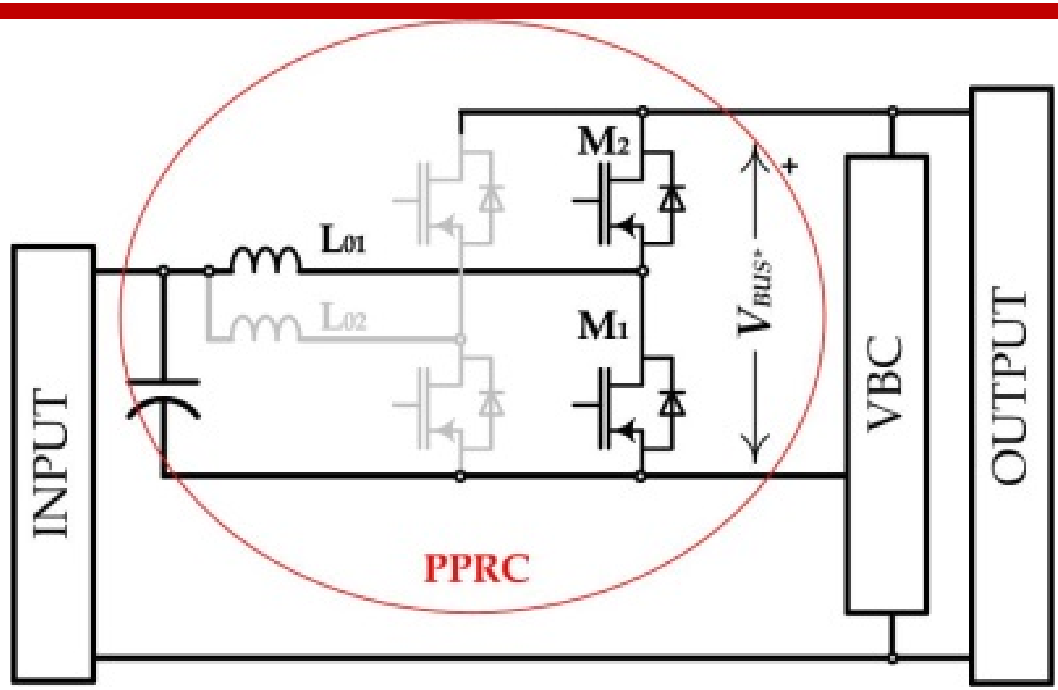


Boost Type



Buck Type

...Partial Power Rated Converters...



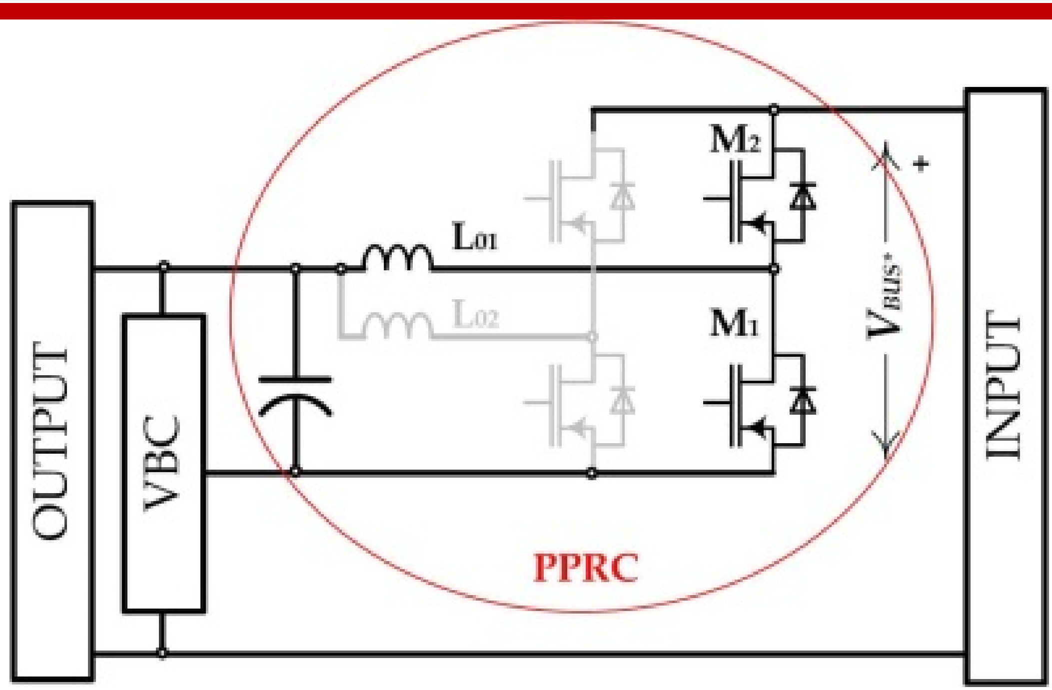
Boost Type Input Partial Power Rated Converter PPRC

- **Internal DC Bus Voltage $_{VBUS*}$ is a fraction of total dc BUS Voltage**

I. Smaller Devices (M1…Mn)

II. Smaller filter inductor L_0

...Partial Power Rated Converters…



Buck Type Input Partial Power Rated Converter PPRC

- **Internal DC Bus Voltage $_{VBUS*}$ is a fraction of total dc BUS Voltage**

I. Smaller Devices (M1…Mn)

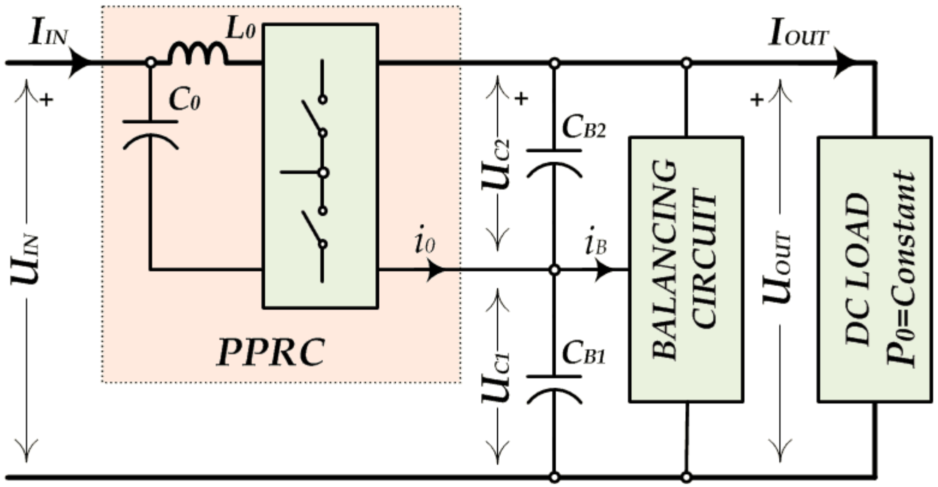
II. Smaller filter inductor L_0

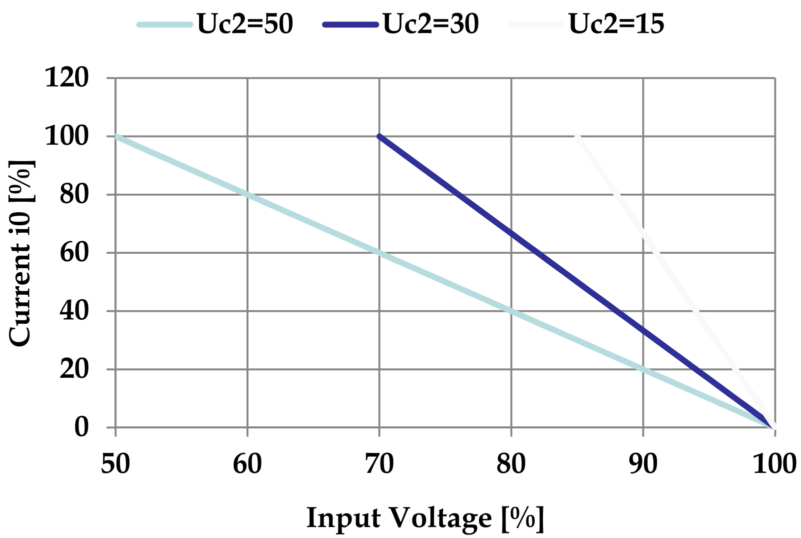
No Meal for Free

- Current i_0 injected in split dc bus caps
- Must be canceled by i_B current

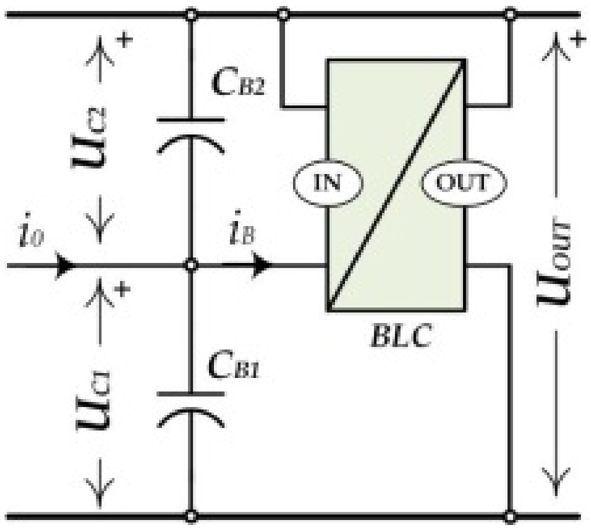
$$i_0 = I_{IN}\frac{U_{OUT} - U_{IN}}{U_{C2}}$$

$$\Downarrow$$

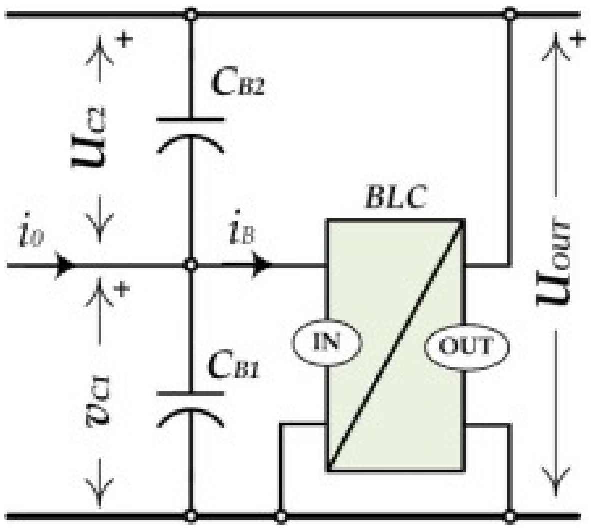




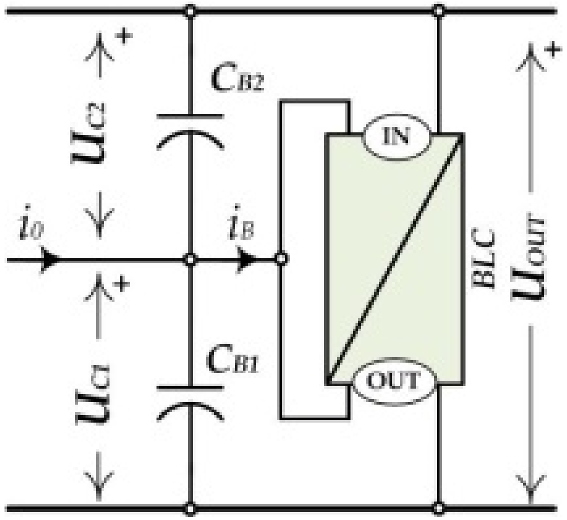
We need another converter : BaLancing Circuit (BLC)

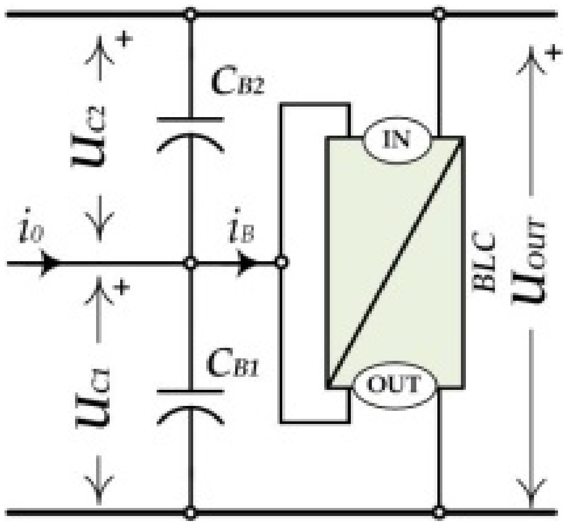


OR

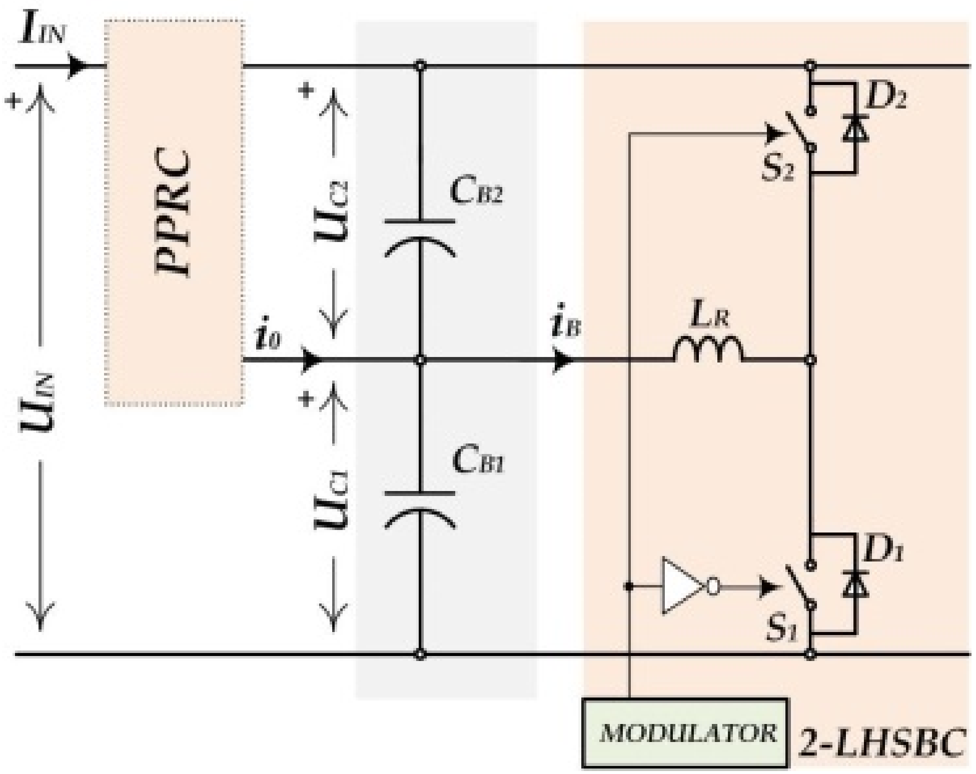


...Partial Power Rated Converters…



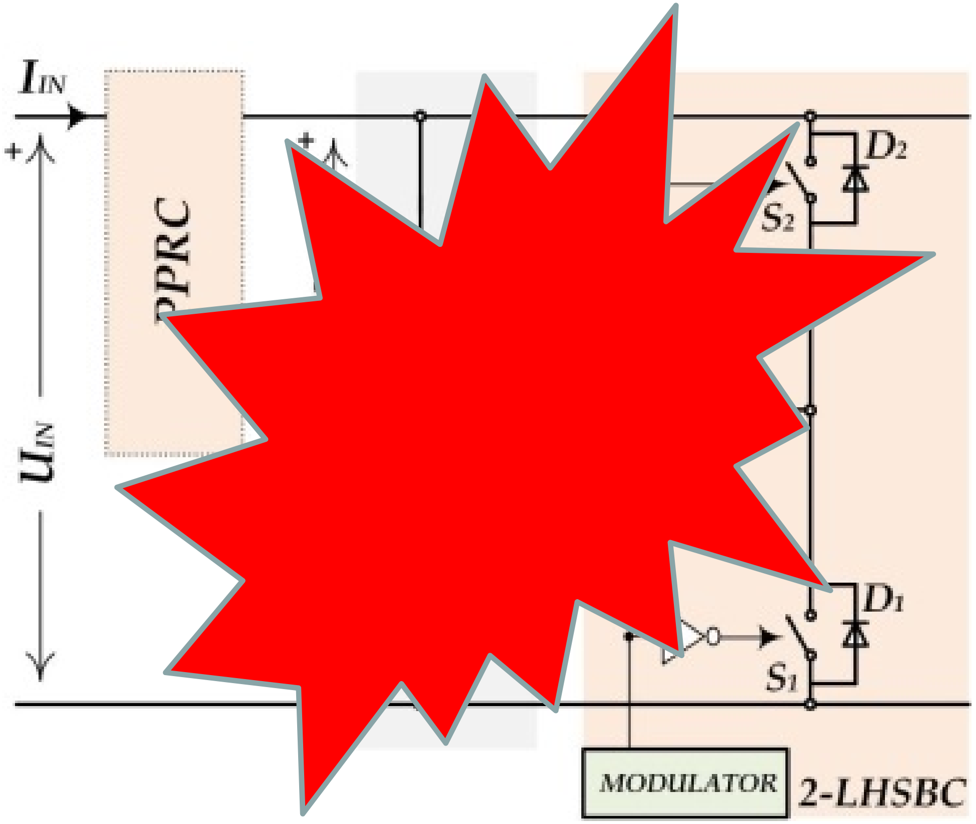


⇒



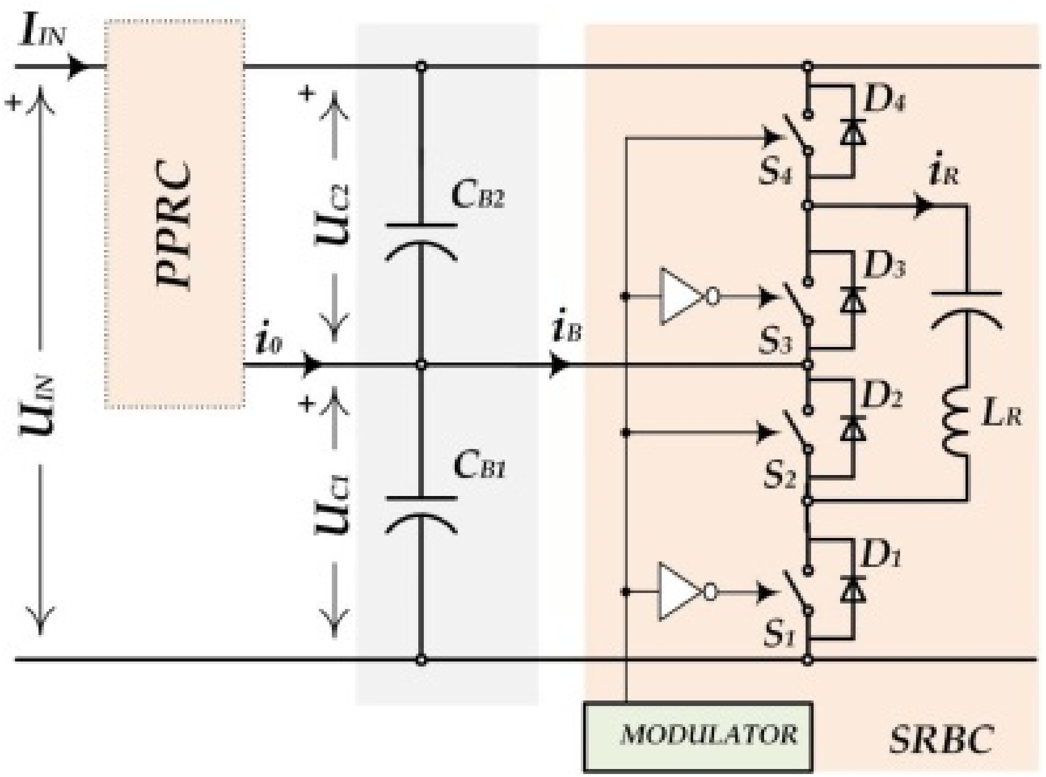
- **Inductor L_R**
- **Switching losses**

...Partial Power Rated Converters...



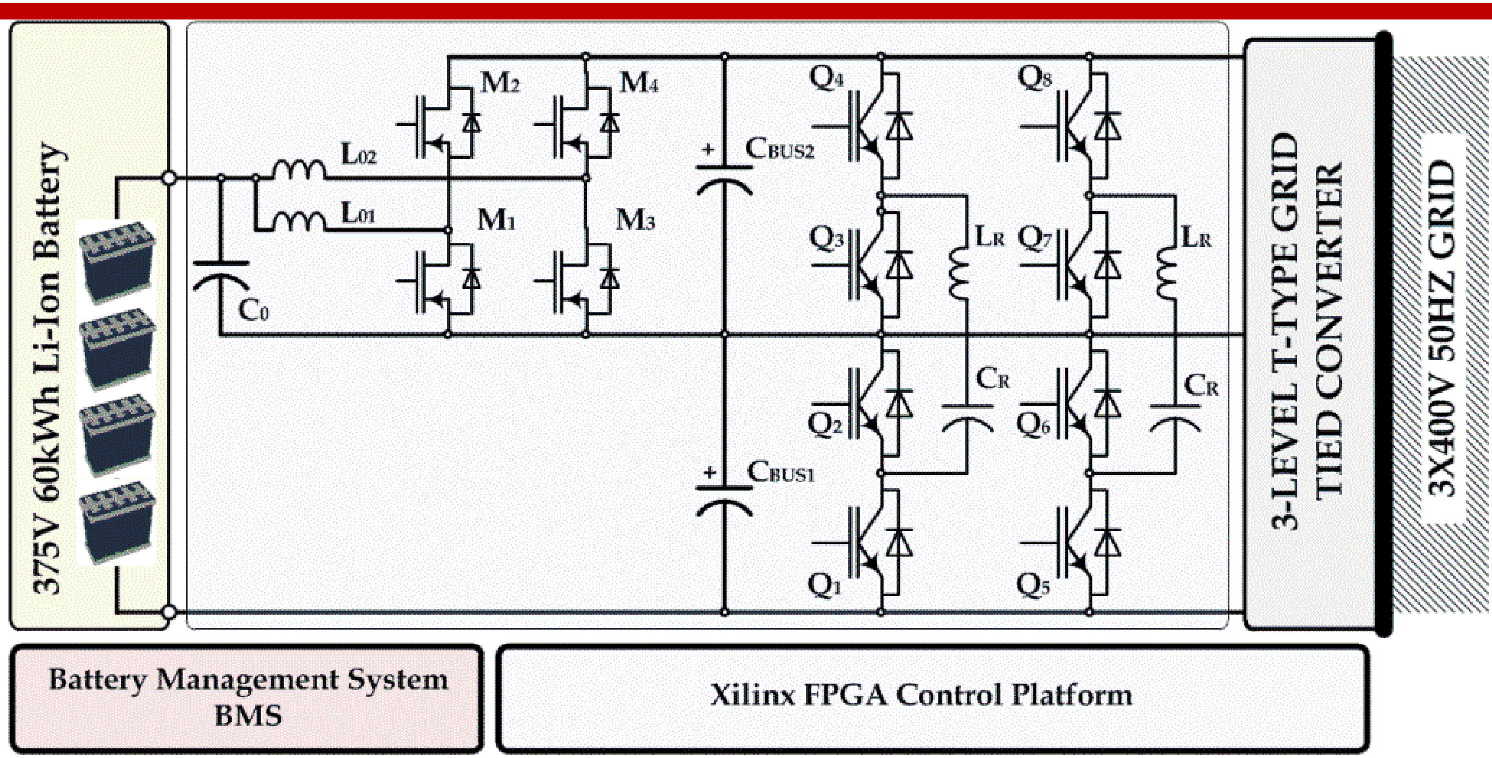
- Inductor L_R
- Switching losses

...Partial Power Rated Converters...



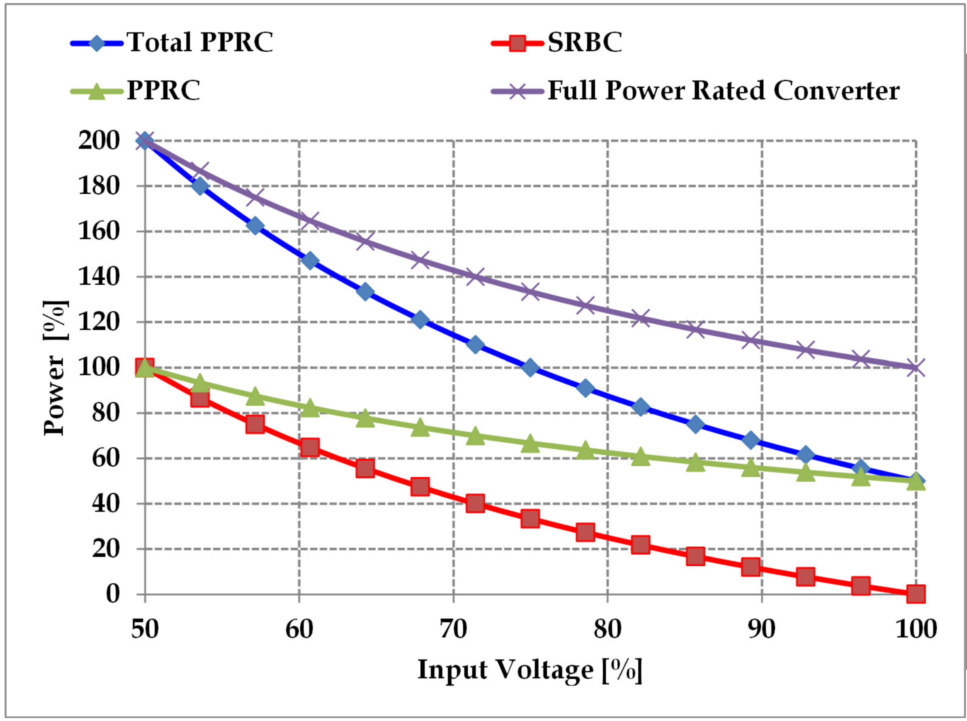
1. **Petar J. Grbović**, Philippe Delarue and Philippe Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter," *IEEE Trans. Industrial Electronics,* Vol. 58, No. 4 pp. 1316-1329, April 2011.
2. Miroslav Vasić, Diego Serrano, Pedro Alou, Jesus A. Oliver, **Petar J. Grbović** and Jose A. Cobos, "Comparative Analysis of Two Compact and Highly Efficient Resonant Switched Capacitor Converters", Accepted for application at Applied Power electronics Conference, APEC 2018, San Antonio, Texas, USA, March 4th to 8th, 2018.

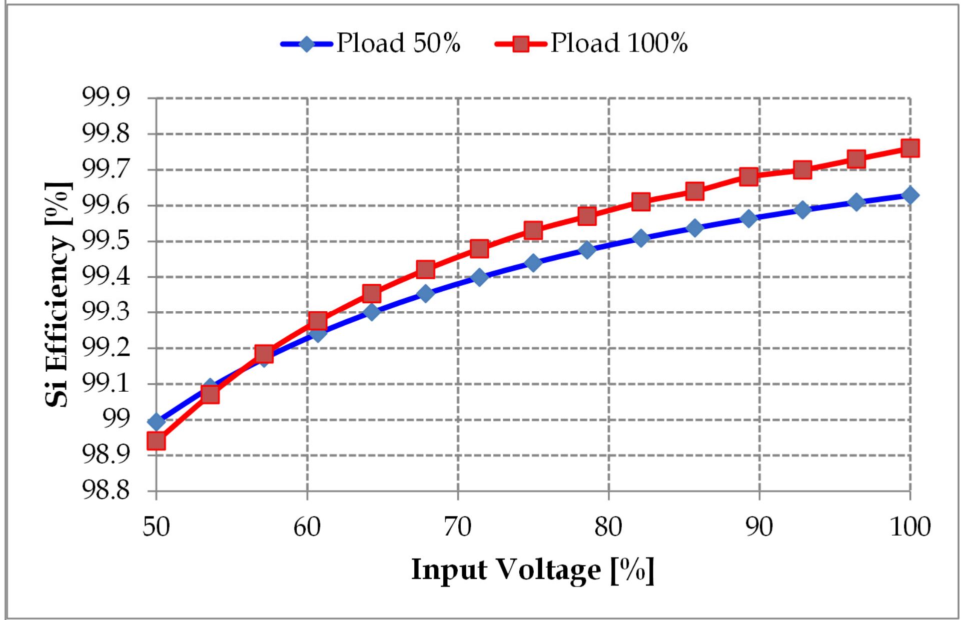
...Partial Power Rated Converters...



- **P. J. Grbović and J. A. Cobos**, "Partial Power Rated DC/DC Converters: A Way to Go Beyond the Limits"
  - 99.5% Efficiency
  - 50kW/dm^3 & 25kW/kg
  - Si Only (no WBG)!!

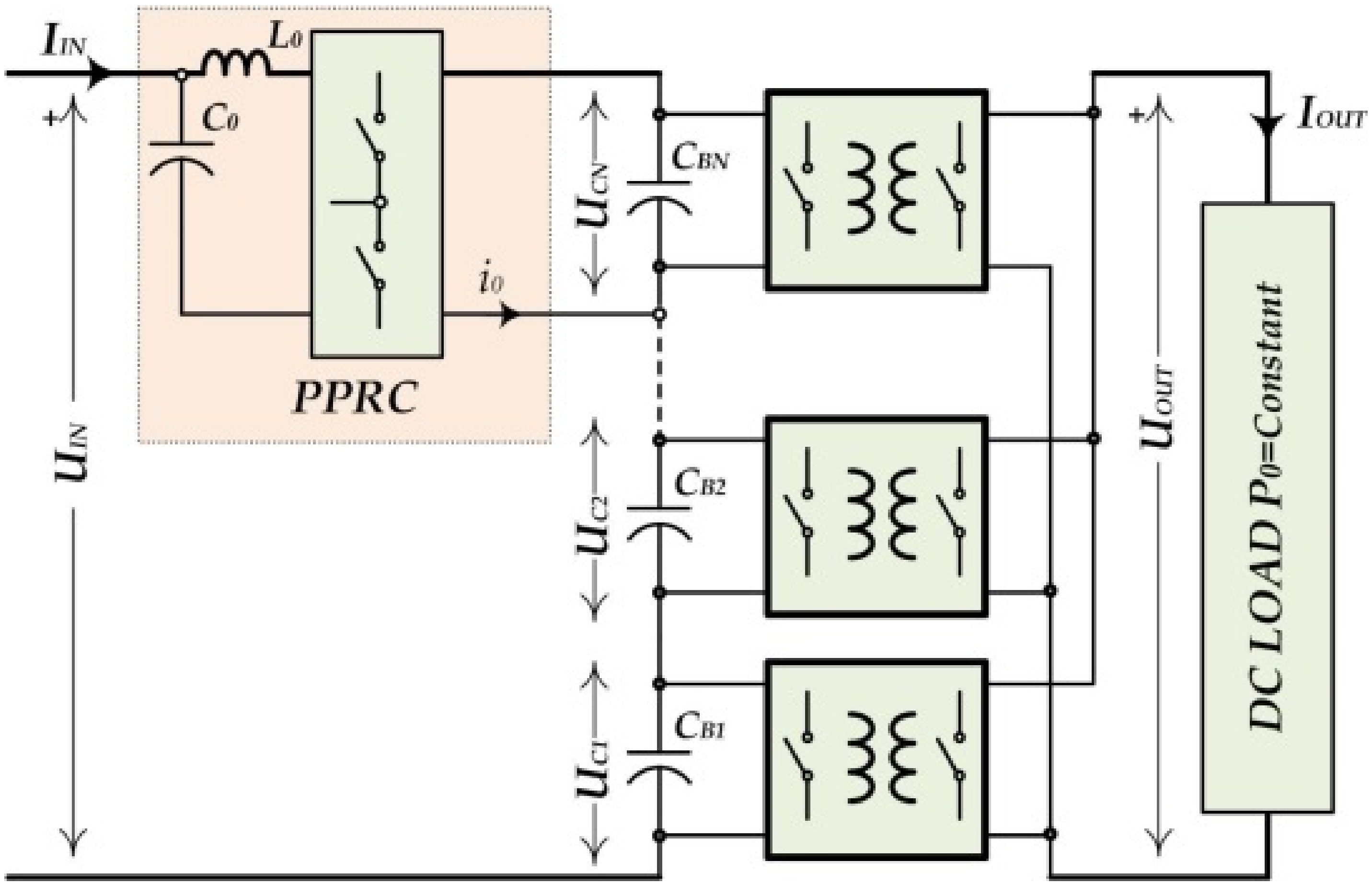
...Partial Power Rated Converters...





- **P. J. Grbović and J. A. Cobos**, "Partial Power Rated DC/DC Converters: A Way to Go Beyond the Limits"
  - 99.5% Efficiency
  - 50kW/dm^3 & 25kW/kg
  - Si Only (no WBG)!!

...Partial Power Rated Converters...

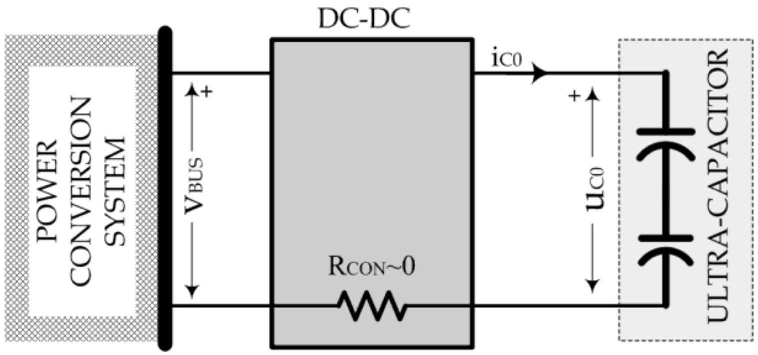


The BLC is the 2nd stage ISOP Converter

Non-Isolated vs. Isolated Converters

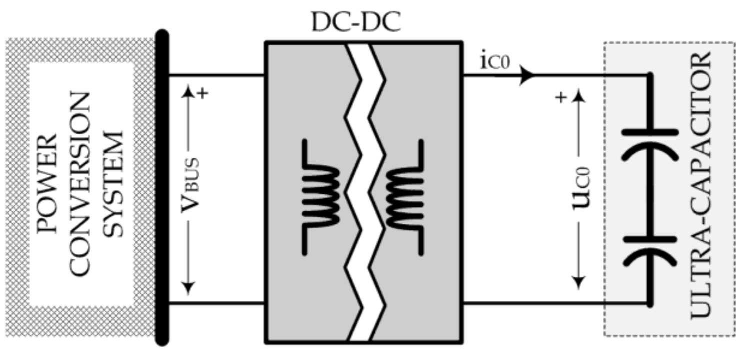
E. Non-isolated dc-dc converter

•Galvanic connection between the input and output



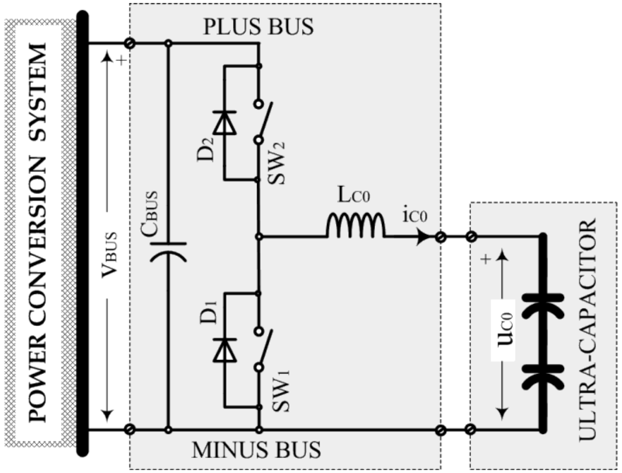
F. Isolated dc-dc converter

•The converter input and output coupled via a high frequency transformer



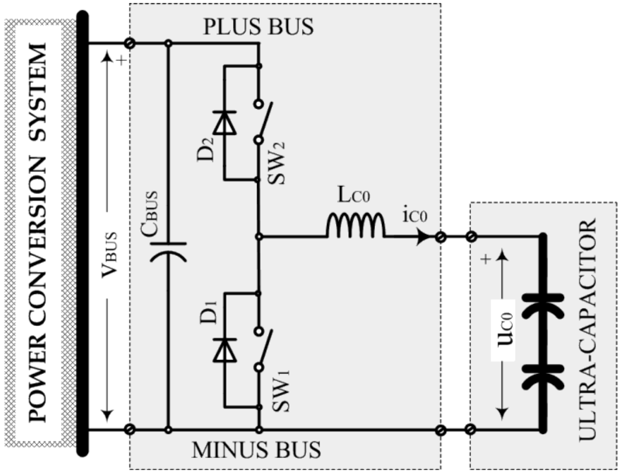
Multi-Cell Converters

1. Single-Cell buck convertor
   - Simple topology
   - The voltage gain $m \leq 1$
   - Full dc bus voltage rating
   - High switching loses
   - Limited switching frequency

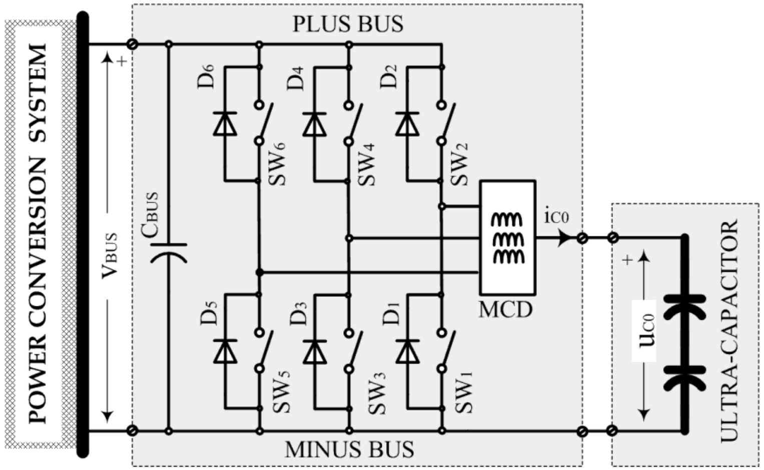


Single-Cell or Multi-Cell Converters

1. Single-Cell buck convertor
   - Simple topology
   - The voltage gain ***m≤1***
   - Full dc bus voltage rating
   - High switching loses
   - Limited switching frequency



2. Multi-Cell interleaved buck convertor
   - Parallel connected ***n*** single phase modules with shifted switching
   - The output current ripple ***1/n***
   - The inductor ripple high
   - Low switching losses
   - The inductor losses are high



Multi-Cell Interleaved Converters

-Split the load current into segments-

...Multi-Cell Converters…

Why we need to split the load (output) current into segments?

I. Good topic for (university) research,

II. Can we do something for passives (Inductors & Capacitors)?

III. Something else?

IV. And, is it a logical step?

...Multi-Cell Converters…

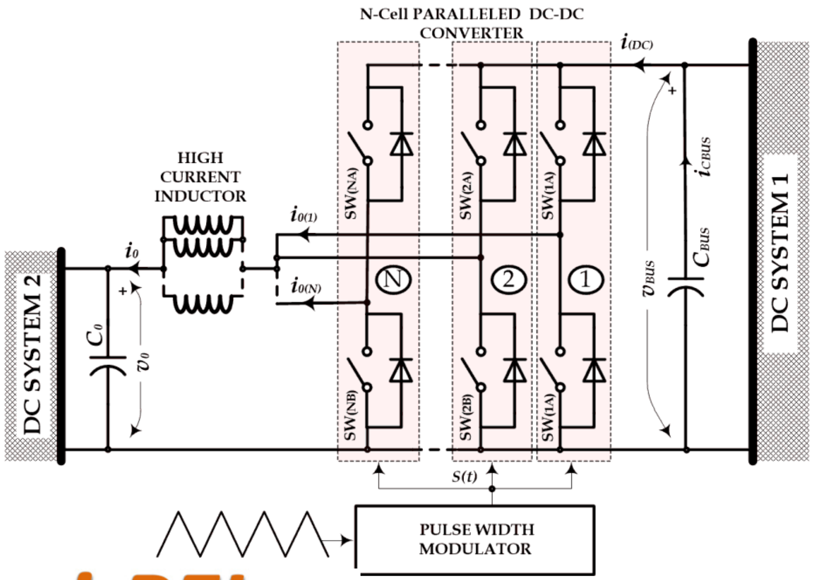
High power (and/or high performances) converters

- ❑ **Paralleling of power semiconductors is a need**

High power (and/or high performances) converters

- ❑ Paralleling of power semiconductors is a need

1. **Direct Paralleling**
   - ❑ Easy control, but
   - ❑ The current sharing is an issues..
   - ❑ No additional benefits

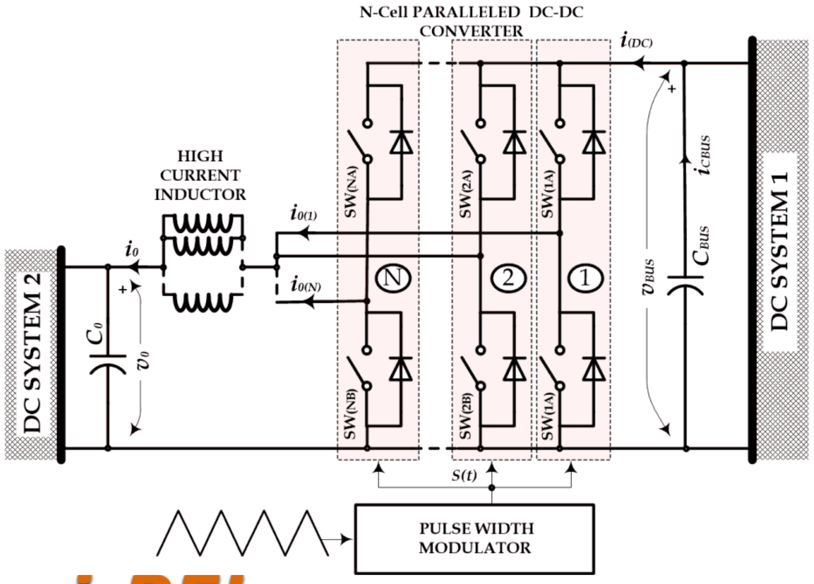


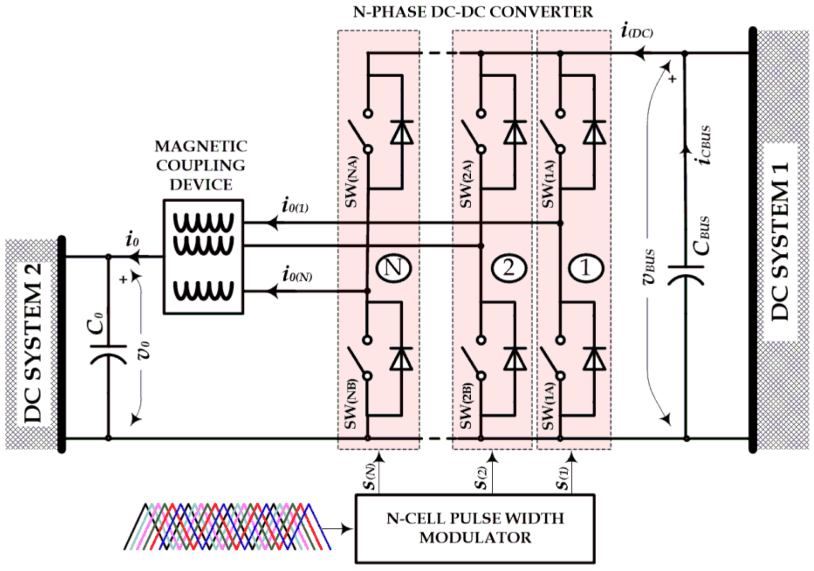
High power (and/or high performances) converters

❑ Paralleling of power semiconductors is a need

1. **Direct Paralleling**
   - ❑ Easy control, but
   - ❑ The current sharing is an issues..
   - ❑ No additional benefits

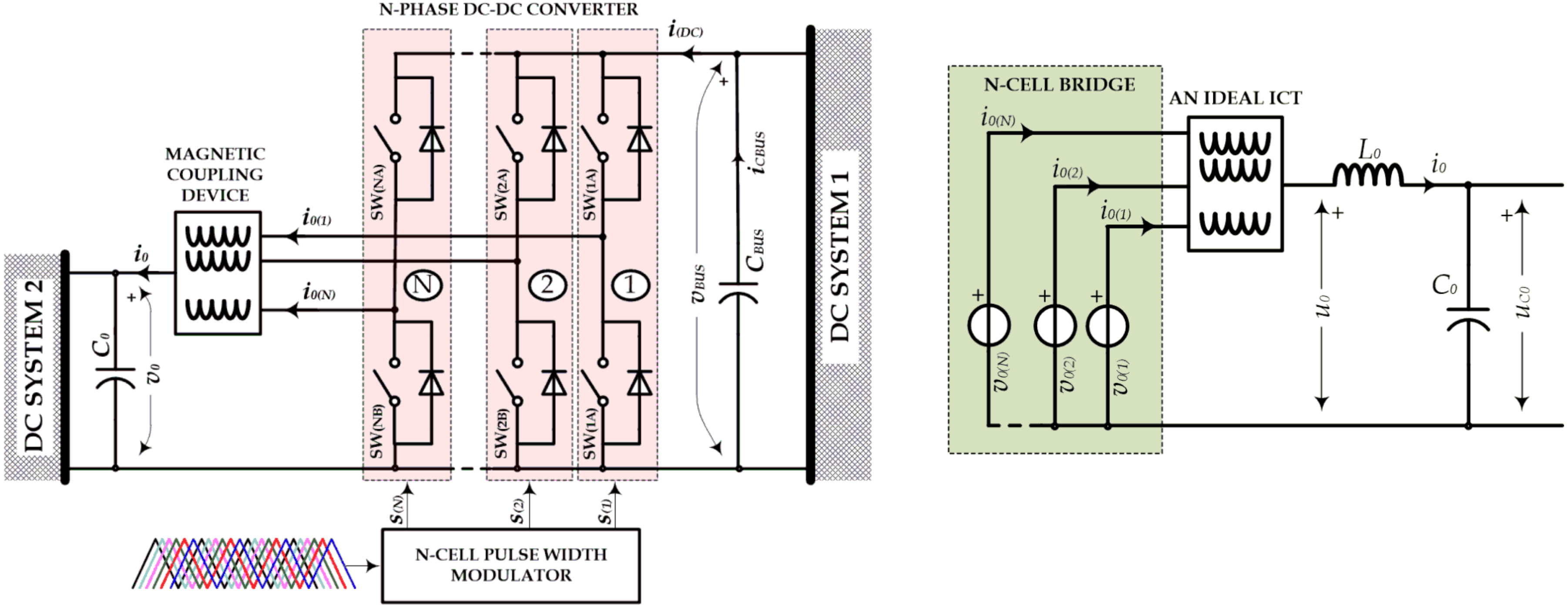
2. **Paralleling with Interleaving**
   - ❑ More expensive, but
   - ❑ Better performances (filter size/cost, losses, control…)





...Multi-Cell Converters...

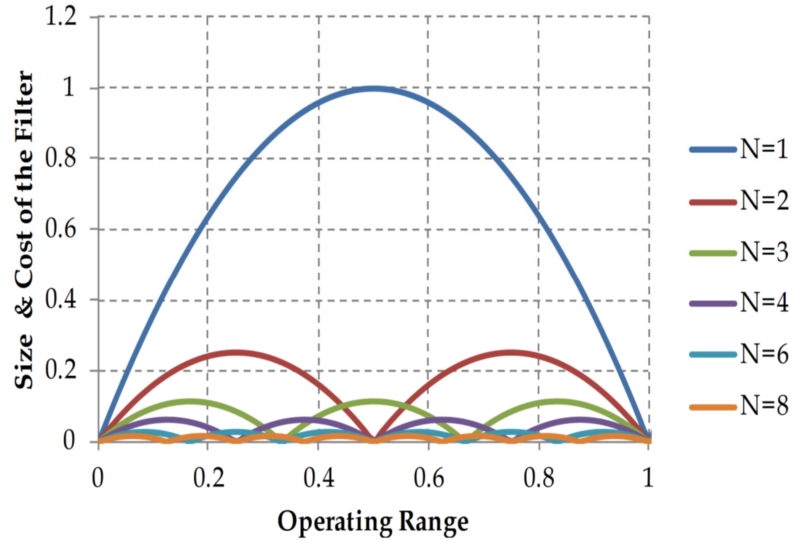
- Intelligent paralleling of devices
- **I**ndividual, **I**ntelligent & **I**nterleaved **C**ontrol -IIIC

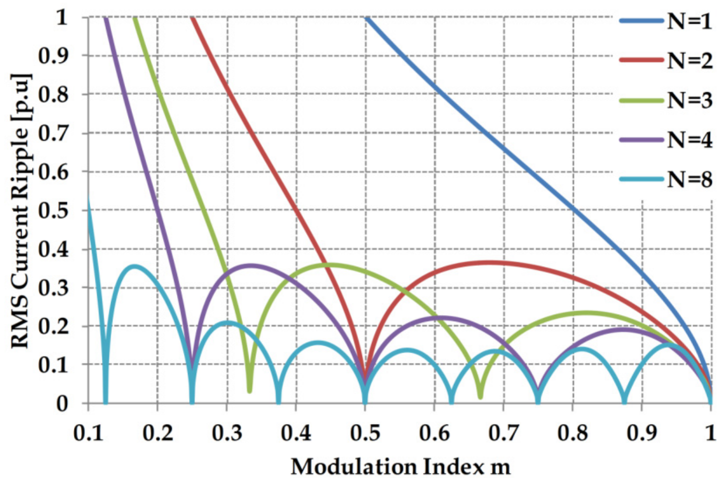


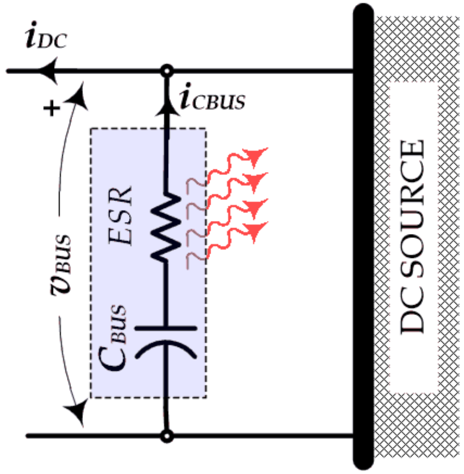
...Multi-Cell Converters…

Harmonics Cancelation

- The input filter cost and size
- The DC Bus Current and DC Bus capacitor stress and losses

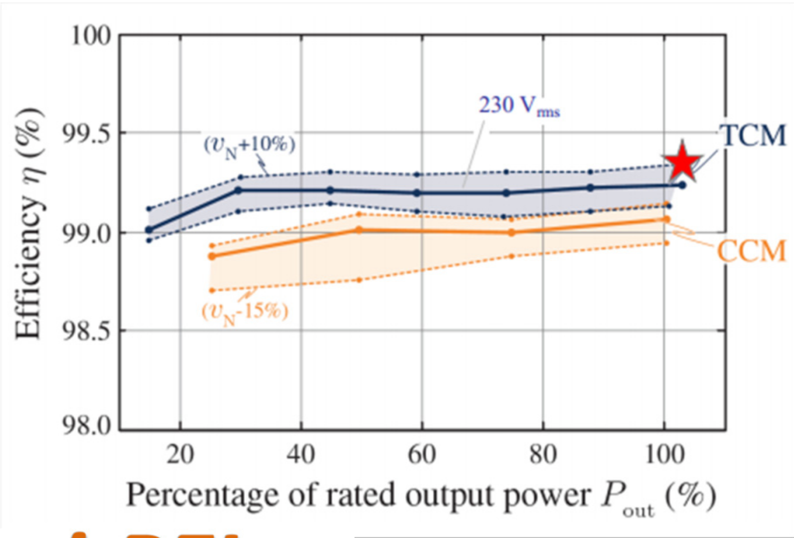


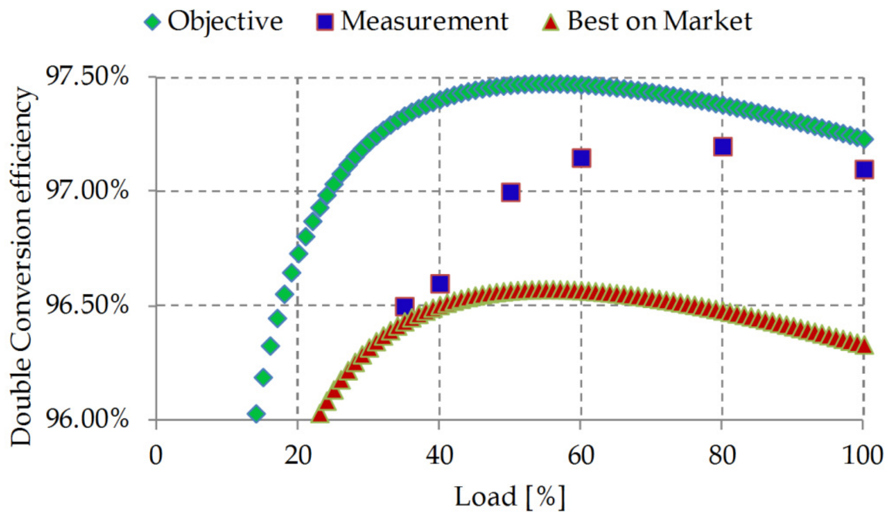




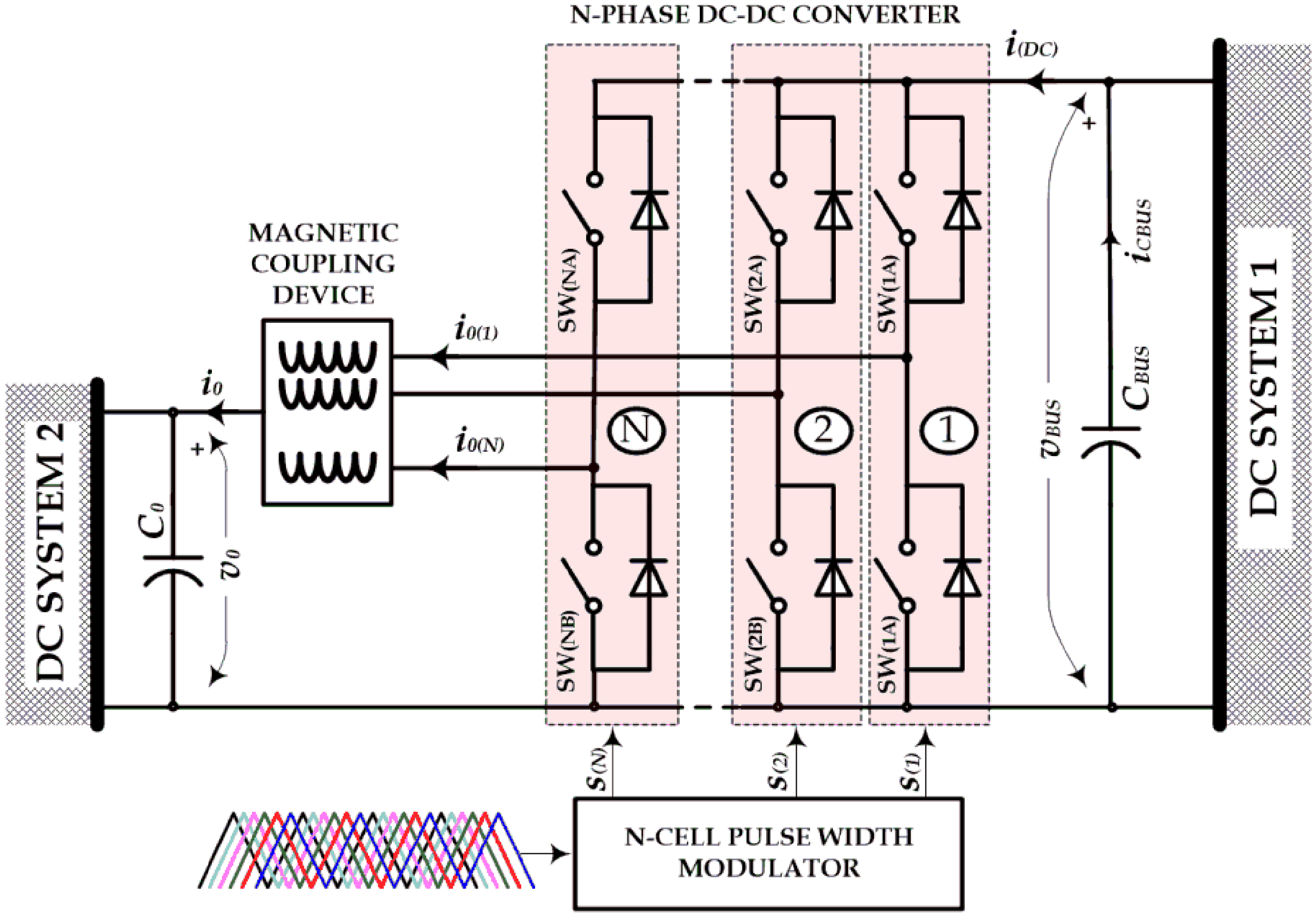
...Multi-Cell Converters…

- 99.3% efficient single phase PFC/Inverter..
  - ETH /Professor J.W. Kolar
- 97.8 % efficient double conversion 100kVA/3U UPS
  - ECCE Huawei Technologies
- All this would not be possible without Interleaving



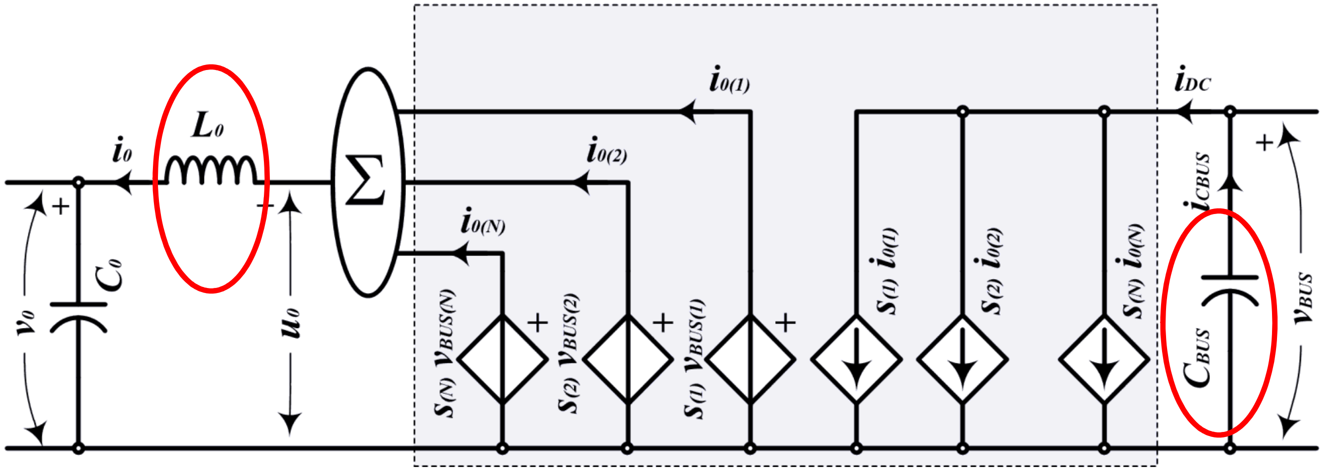


...N-Cell Converter Analysis...



...N-Cell Converter Analysis...

- In General, How does it Work?



- k^{th} cell switching function

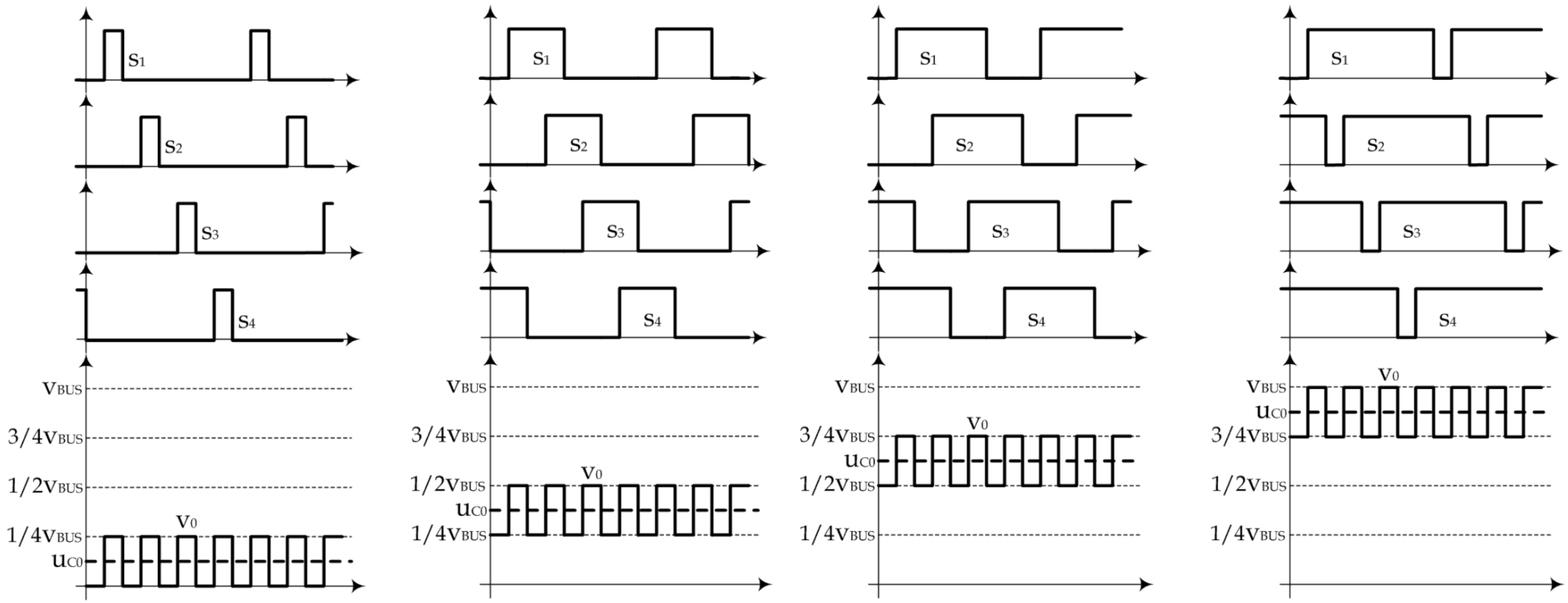
$$s_{(k)}(t) = d + \frac{2}{\pi}\sum_{p=1}^{\infty}\frac{1}{p}\sin(pd\pi)\cos\left(p\omega_{SW}t + \frac{2\pi}{N}(k-1)\right) \qquad k = (1,2,\ldots N)$$

- Output voltage u_0 and dc bus current i_{DC}

$$v_0(t) = \sum_{k=1}^{N}\frac{v_{0(k)}(t)}{N} = \frac{V_{BUS}}{N}\sum_{k=1}^{N}s_k(t) \qquad i_{DC}(t) = \sum_{k=1}^{N}s_{(k)}(t)i_{0(k)}(t)$$

...N-Cell Converter Analysis...

- 4-cell converter example



$0<d<1/4$ $1/4<d<1/2$ $1/2<d<3/4$ $3/4<d<1$

...N-Cell Converter Analysis...

- N-Cell Converter output voltage u_0

1
$$u_0(t) = dV_{BUS} + V_{BUS}\frac{2}{\pi}\sum_{p=1}^{\infty}\left[\frac{1}{p}\sin(pd\pi)\sum_{k=1}^{N}\cos\left(p\omega_{SW}t + \frac{2\pi}{N}(k-1)\right)\right]$$

2a
$$\cos(\alpha+\beta) = \cos(\alpha)\cos(\beta) - \sin(\alpha)\sin(\beta)$$

2b
$$\sum_{k=1}^{N}\cos p\frac{2\pi}{N}(k-1) = \begin{cases} 1 & p = iN \\ 0 & p \neq iN \end{cases} \quad i = \{1..\infty\}$$

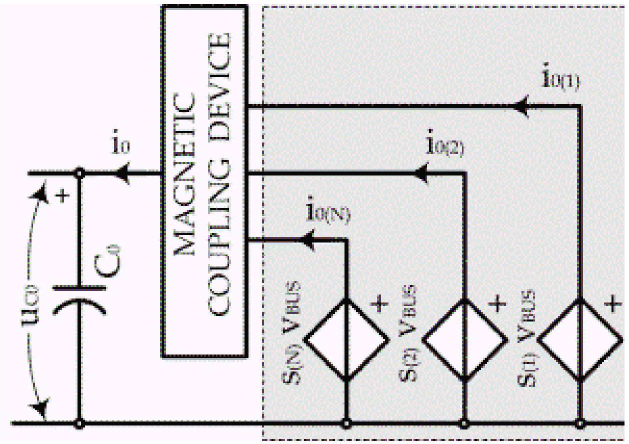
2c
$$\sum_{k=1}^{N}\sin p\frac{2\pi}{N}(k-1) = 0$$

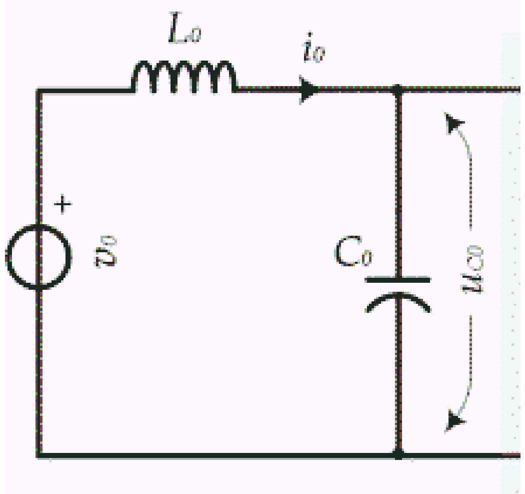
- All harmonics up to N^{th} are canceled from the output voltage

3
$$u_0(t) = dV_{BUS} + \frac{V_{BUS}}{N}\frac{2}{\pi}\sum_{i=1}^{\infty}\left[\frac{1}{i}\sin(iNd\pi)\cos(iN\omega_{SW}t)\right]$$

- Similar applies to the dc bus current i_{CBUS}

...N-Cell Converter Analysis...





$$L_0 \frac{di_0}{dt} = v_0(t) - u_{C0}$$

$$\Delta i_0(t) = \frac{\Delta i_0(d)}{2} \begin{cases} -1 + N \dfrac{\Delta i_0(d)}{dT_{sw}} t & 0 \le t \le d \dfrac{T_{sw}}{N} \\ 1 - N \dfrac{\Delta i_0(d)}{(1-d)T_{sw}} \left(t - d \dfrac{T_{sw}}{N} \right) & d \dfrac{T_{sw}}{N} \le t \le \dfrac{T_{sw}}{N} \end{cases}$$

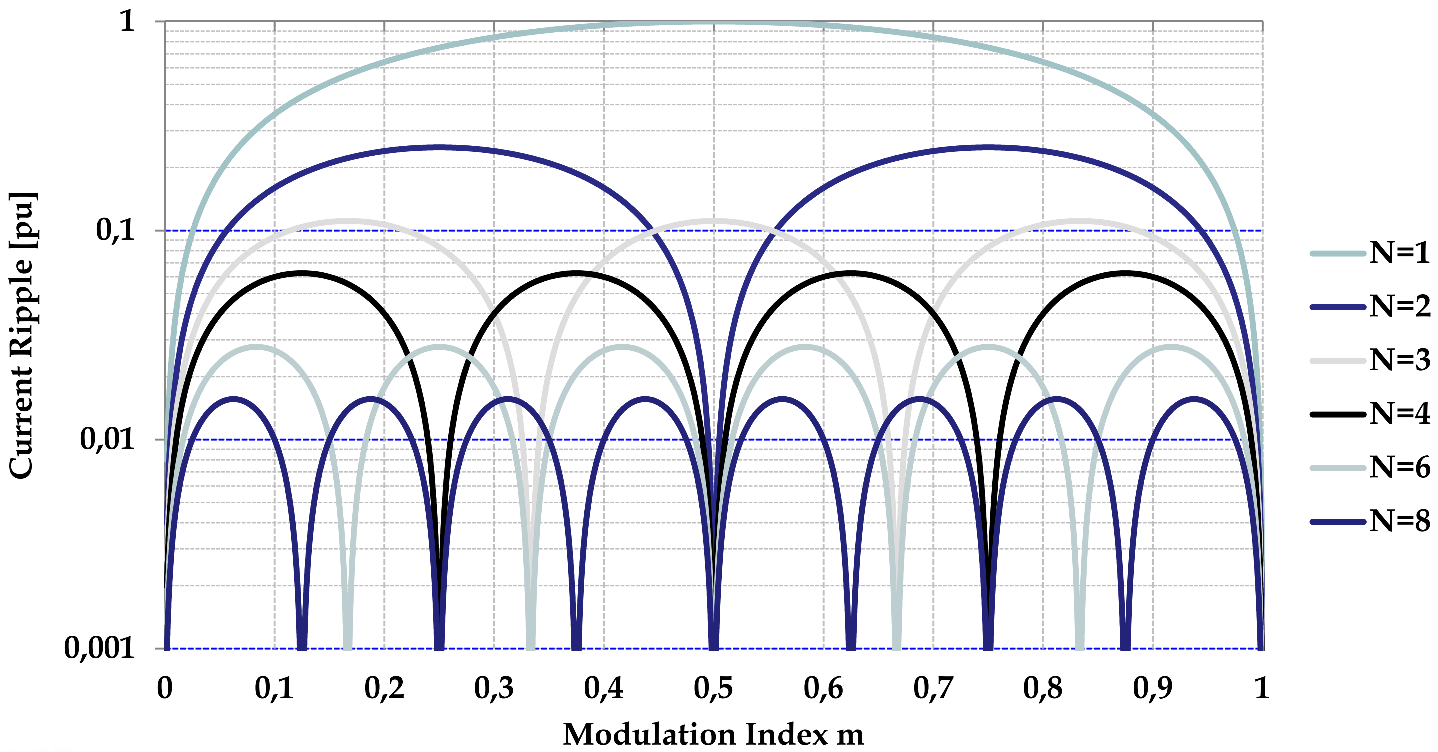
- The Inductor Current Ripple

$$\Delta i_0(d) = \left(\frac{V_{BUS}}{4 f_{SW} L_0} \right) \frac{4}{N^2} \left[(Nd - floor(Nd)) - (Nd - floor(Nd))^2 \right] = \left(\frac{V_{BUS}}{4 f_{SW} L_0} \right) K_{\Delta i}(d)$$

...N-Cell Converter Analysis...

- The Inductor Current Ripple…..

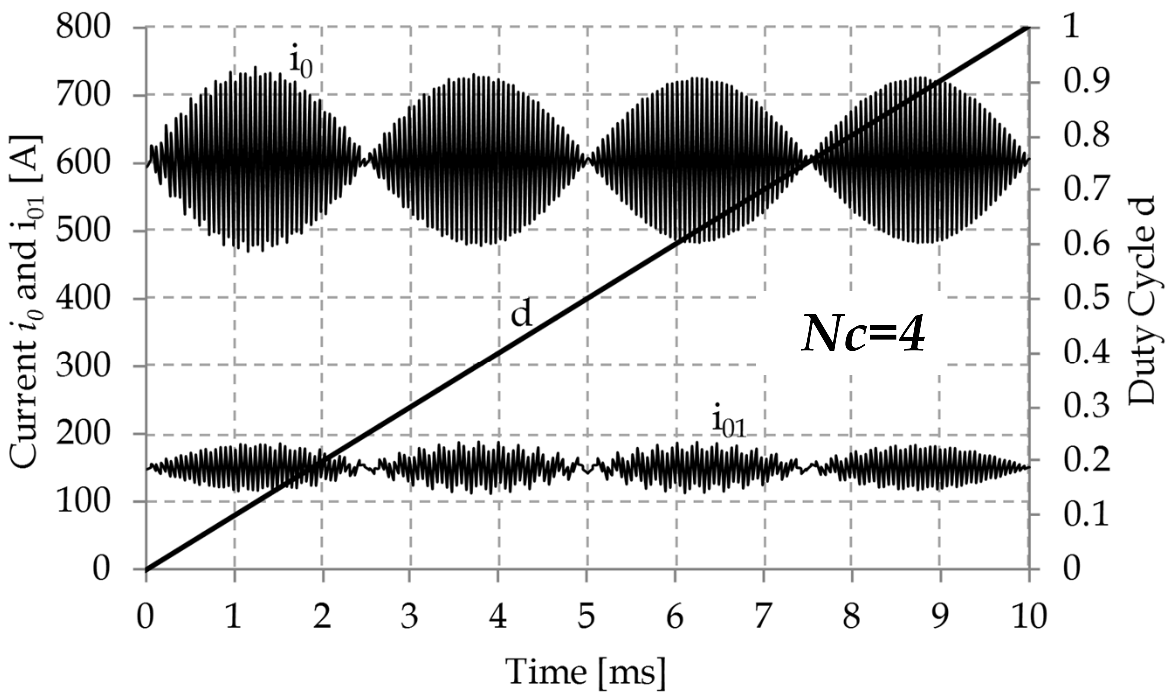
$$\Delta i_0(d)=\left(\frac{V_{BUS}}{4f_{SW}L_0}\right)\frac{4}{N^2}\left[\left(Nd-floor(Nd)\right)-\left(Nd-floor(Nd)\right)^2\right]=\left(\frac{V_{BUS}}{4f_{SW}L_0}\right)K_{\Delta i}(d)$$



...N-Cell Converter Analysis...

- The Inductor Current Ripple.....

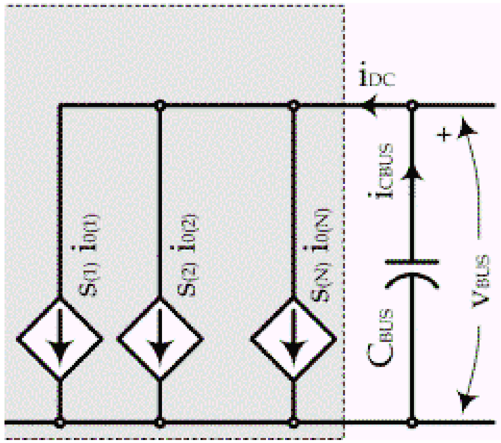
$$\Delta i_0(d)=\left(\frac{V_{BUS}}{4 f_{SW} L_0}\right)\frac{4}{N^2}\left[\left(Nd-floor(Nd)\right)-\left(Nd-floor(Nd)\right)^2\right]=\left(\frac{V_{BUS}}{4 f_{SW} L_0}\right)K_{\Delta i}(d)$$

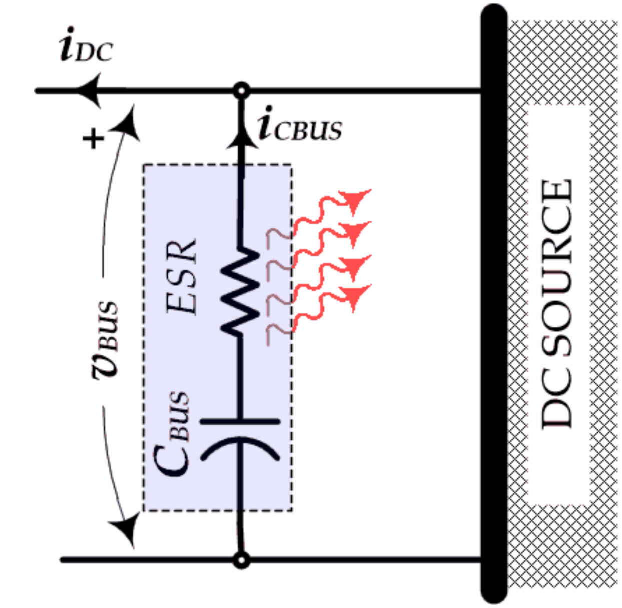


...N-Cell Converter...

DC Bus Current i_{DC}

- Capacitor stress
- Losses
- Voltage Ripple
- **The Cap. Size/cost**





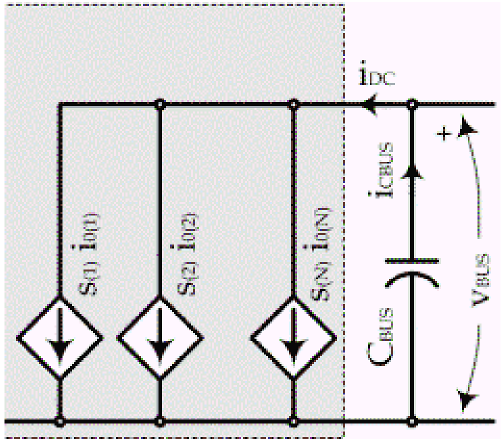
$$i_{DC}(t)=\sum_{k=1}^{N}s_{(k)}(t)i_{OUT(k)}(t)$$

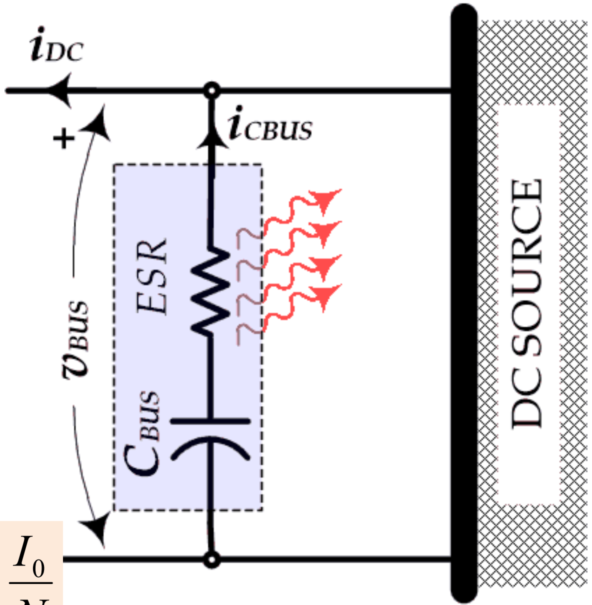
$$i_{(DC)}(t)=\sum_{k=1}^{N}d_{(k)}I_{0(k)}+\sum_{k=1}^{N}I_{0(k)}\frac{2}{\pi}\sum_{p=1}^{\infty}\frac{1}{p}\sin(pd\pi)\cos\left(p\omega_{SW}t+\frac{2\pi}{N}(k-1)\right)+\sum_{k=1}^{N}d_{(k)}\Delta i_{0(k)}(t)$$

$$+\underbrace{\sum_{k=1}^{N}\Delta i_{0(k)}(t)\frac{2}{\pi}\sum_{p=1}^{\infty}\frac{1}{p}\sin(pd\pi)\cos\left(p\omega_{SW}t+\frac{2\pi}{N}(k-1)\right)}_{\cong 0}$$

DC Bus Current i_{DC}

- Capacitor stress
- Losses
- Voltage Ripple
- **The Cap. Size/cost**





$$i_{DC}(t)=\sum_{k=1}^{N} s_{(k)}(t)i_{OUT(k)}(t)$$

$$d_{(1)}=\ldots=d_{(N)}=d \ \& \ I_{0(1)}=..=I_{0(N)}=\frac{I_0}{N}$$

$$\Delta i_{0(1)}(t)=\Delta i_{0(2)}=..=\Delta i_{0(N)}(t)=\frac{\Delta i_0(t)}{N}$$

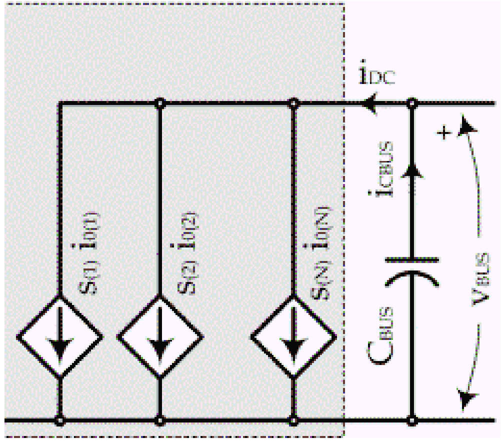
$$i_{(DC)}(t)\cong dI_0+I_0\frac{2}{\pi}\sum_{p=1}^{\infty}\left[\frac{1}{p}\sin(pd\pi)\sum_{k=1}^{N}\cos\left(p\omega_{SW}t+\frac{2\pi}{N}(k-1)\right)\right]+d\Delta i_0(t)$$

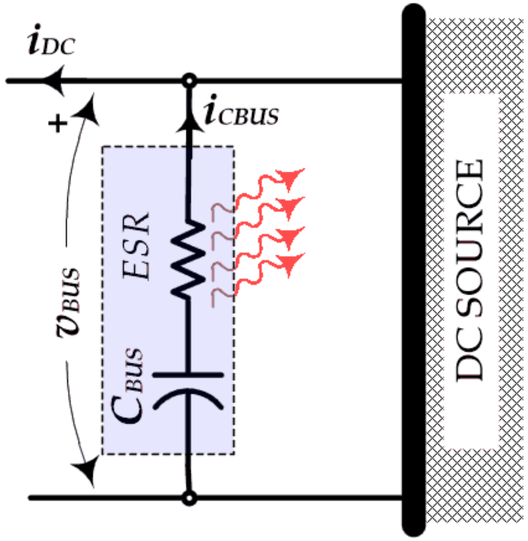
$$=dI_0+\underbrace{\frac{I_0}{N}\frac{2}{\pi}\sum_{i=1}^{\infty}\left[\frac{1}{i}\sin(iNd\pi)\cos(iN\omega_{SW}t)\right]+d\Delta i_0(t)}_{i_{CBUS}(t)}$$

...N-Cell Converter Analysis...

DC Bus Current i_{DC}

- Capacitor stress
- Losses
- Voltage Ripple
- The Cap. Size/cost





RMS Current

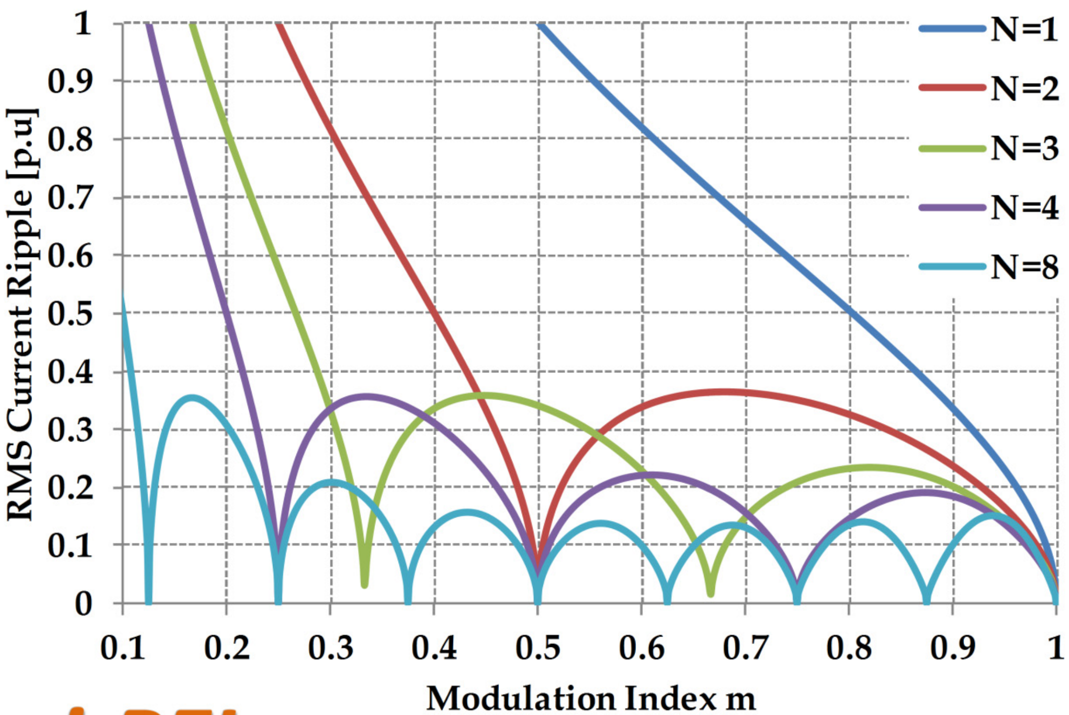
$$I_{CBUS(RMS)} = \sqrt{\frac{1}{T}\int_0^T i_1^2(t)dt + \frac{1}{T}\int_0^T i_2^2(t)dt + \underbrace{\frac{1}{T}\int_0^T i_1 i_2(t)dt}_{=0}} = \sqrt{\left(\frac{I_0}{N}\frac{\sqrt{2}}{\pi}\right)^2 \sum_{i=1}^{\infty}\frac{1}{i^2}\sin^2(iNd\pi) + d^2\Delta i_{0(RMS)}^2}$$

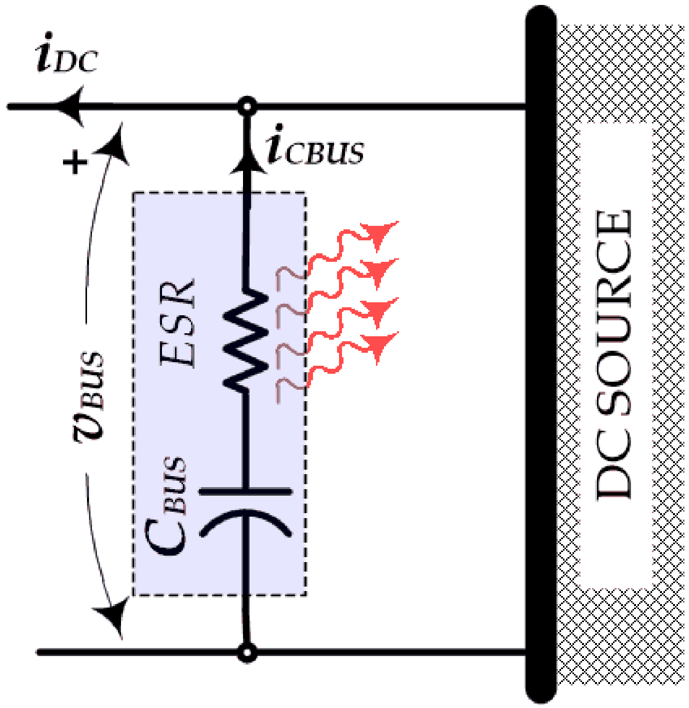
Petar J. Grbović, "Closed Form Analysis of N-Cell Interleaved Two-Level DC-DC Converters: The DC Bus Capacitor Current Stress Analysis," ECCE Asia 2013, Down Under, IEEE Energy Conversion Congress and Exposition, Melbourne, Australia, 3-6 June, 2013.

...N-Cell Converter Analysis...

RMS Current

$$I_{CBUS(RMS)} = \frac{P_{C0}}{V_{BUS}} \sqrt{ \frac{\left[\left(Nm - floor(Nm) \right) - \left(Nm - floor(Nm) \right)^2 \right]}{(Nm)^2} + \left(\frac{V_{BUS}}{P_{C0}} \Delta i_{0(\max)} m \frac{2}{\sqrt{3}} \right)^2 \left[\left(Nm - floor(Nm) \right) - \left(Nm - floor(Nm) \right)^2 \right]^2 }$$

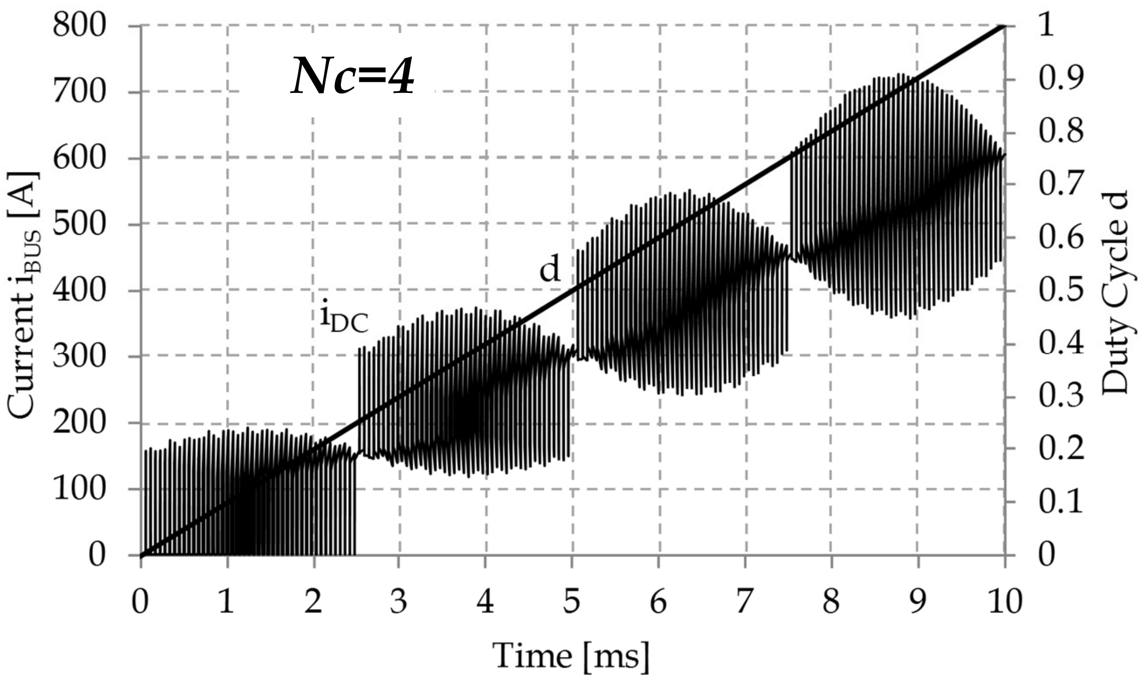


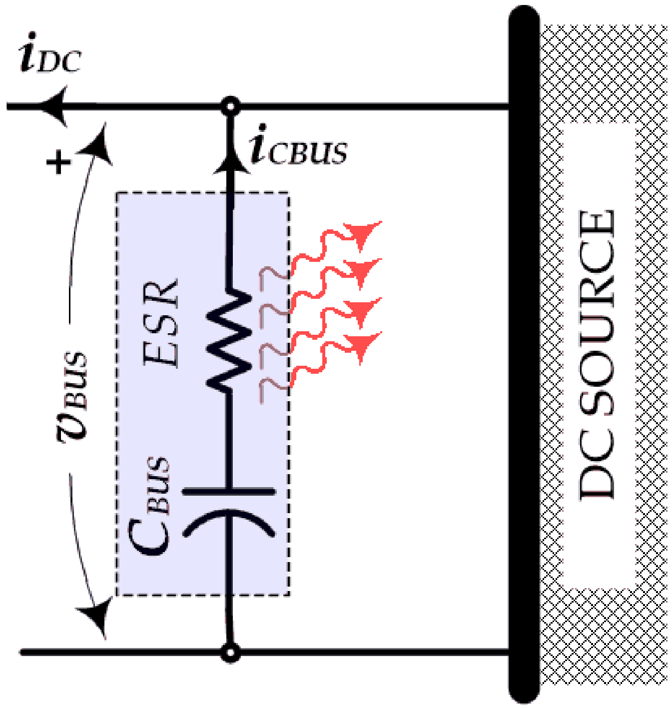


...N-Cell Converter Analysis...

RMS Current

$$I_{CBUS(RMS)} = \frac{P_{C0}}{V_{BUS}} \sqrt{ \frac{\left[(Nm - floor(Nm)) - (Nm - floor(Nm))^2 \right]}{(Nm)^2} + \left(\frac{V_{BUS}}{P_{C0}} \Delta i_{0(\max)} m \frac{2}{\sqrt{3}} \right)^2 \left[(Nm - floor(Nm)) - (Nm - floor(Nm))^2 \right]^2 }$$

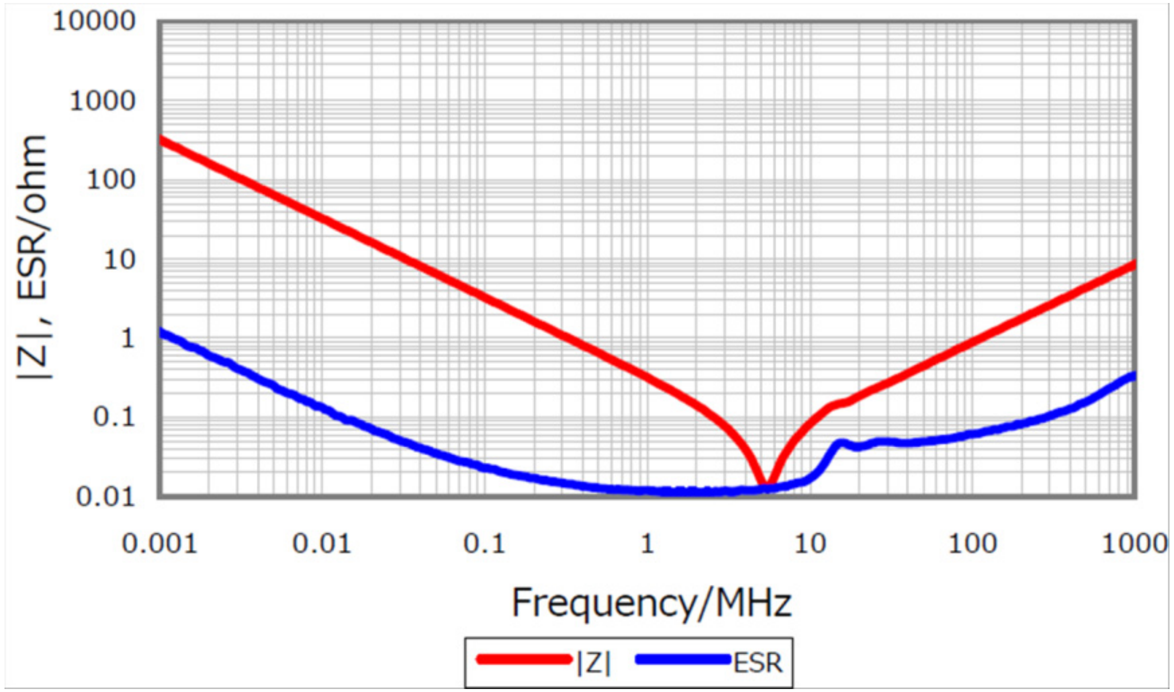




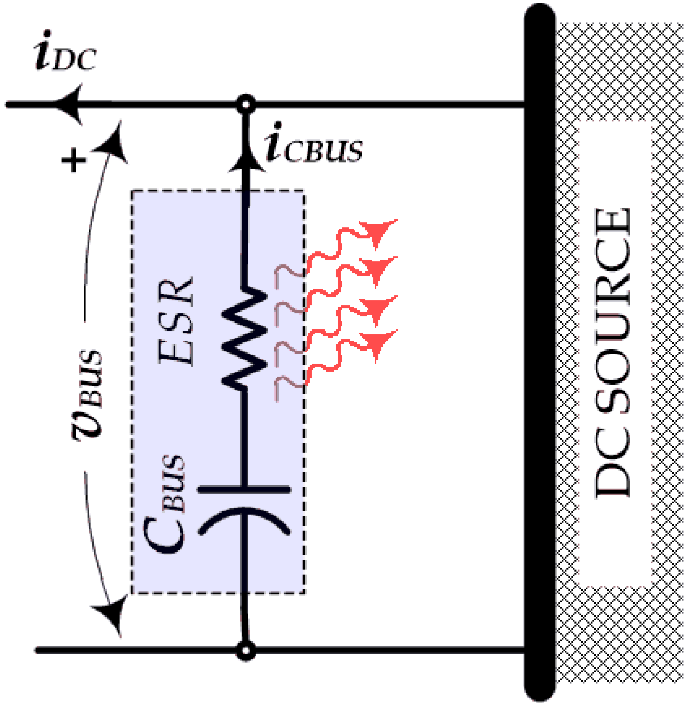
...N-Cell Converter Analysis...

RMS Current

$$I_{CBUS(RMS)} = \frac{P_{C0}}{V_{BUS}} \sqrt{\frac{\left[(Nm - floor(Nm)) - (Nm - floor(Nm))^2 \right]}{(Nm)^2} + \left(\frac{V_{BUS}}{P_{C0}} \Delta i_{0(\max)} m \frac{2}{\sqrt{3}} \right)^2 \left[(Nm - floor(Nm)) - (Nm - floor(Nm))^2 \right]^2}$$



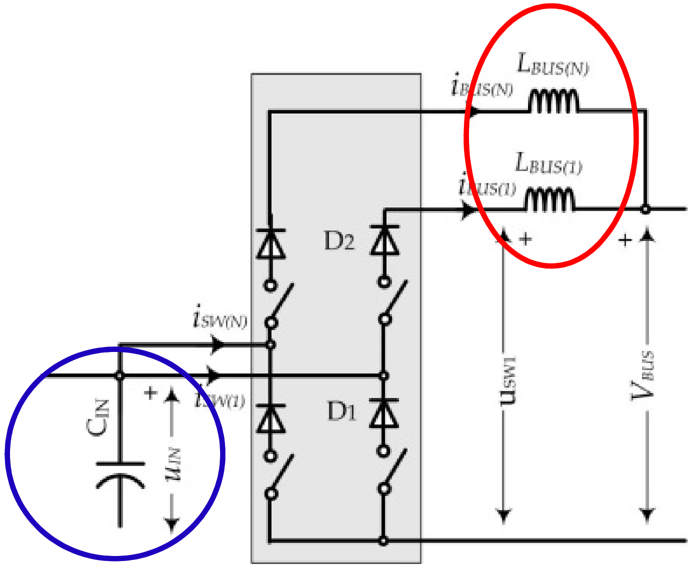
MLCC

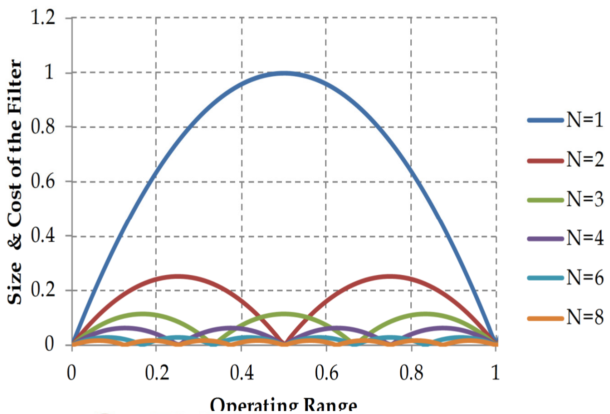


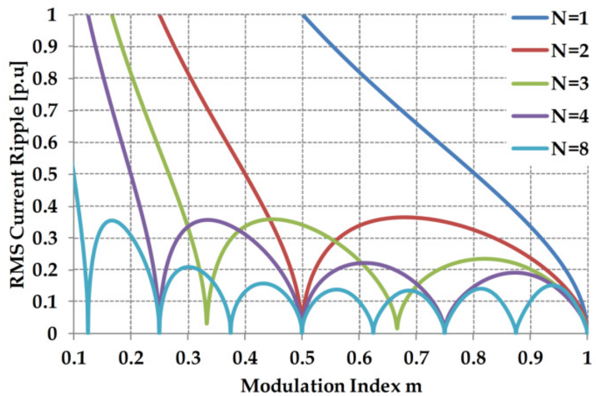
...N-Cell CSC...

Go back to CSC

- **Input Capacitor & Current Stress!!**
- **N-Cell Interleaved CSC**
  - **Small Grid Side Filter Capacitor...**
  - **Small DC Bus Inductors**



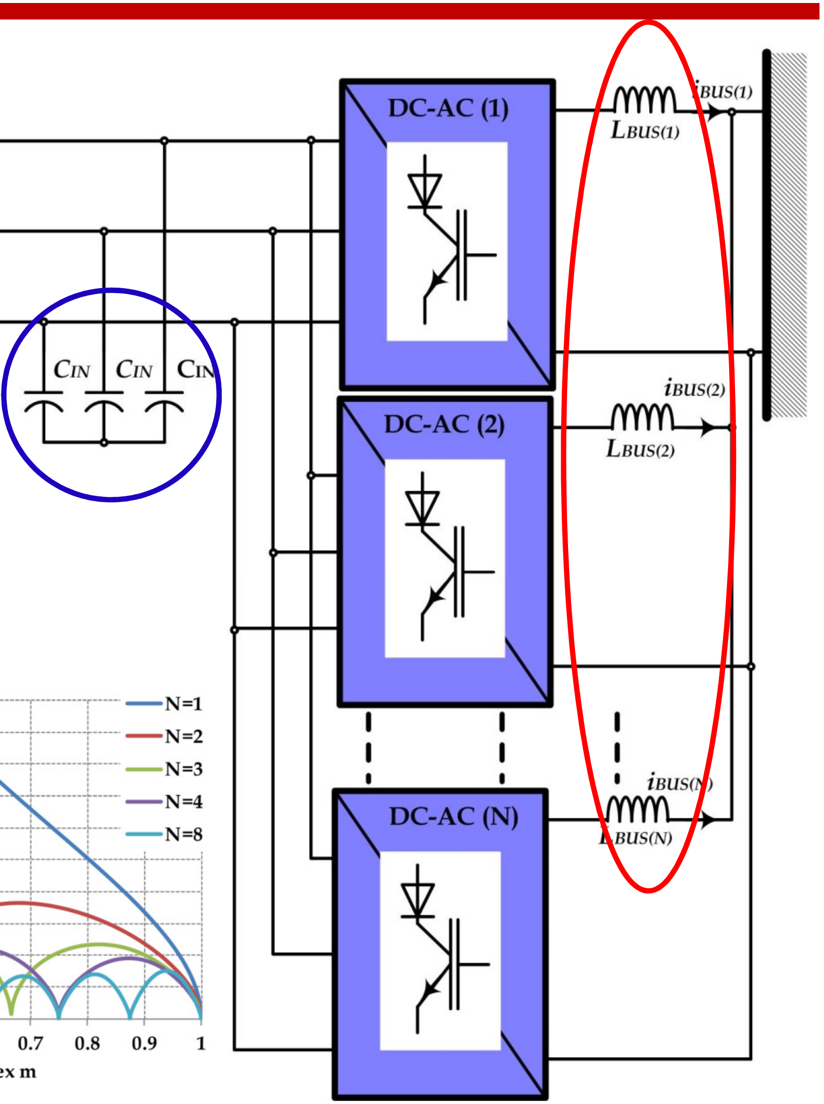


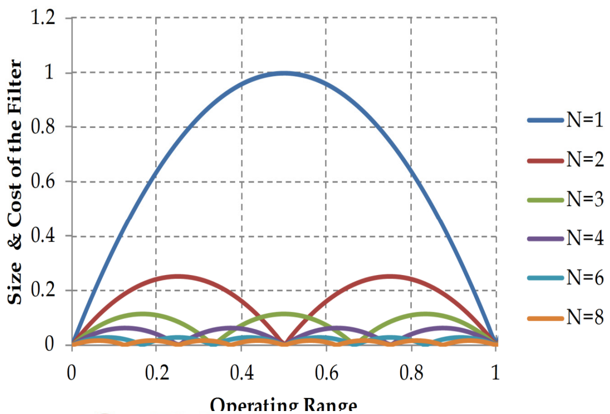


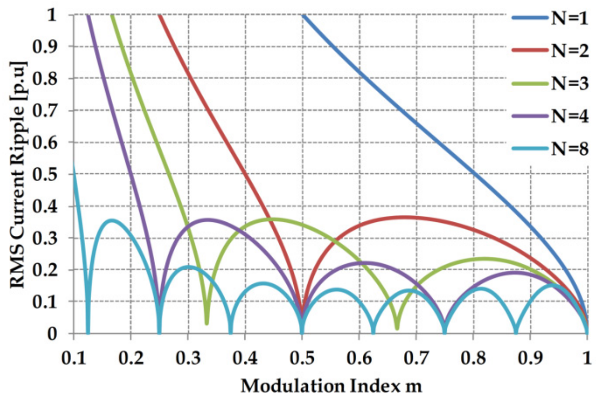
...N-Cell CSC...

Go back to CSC

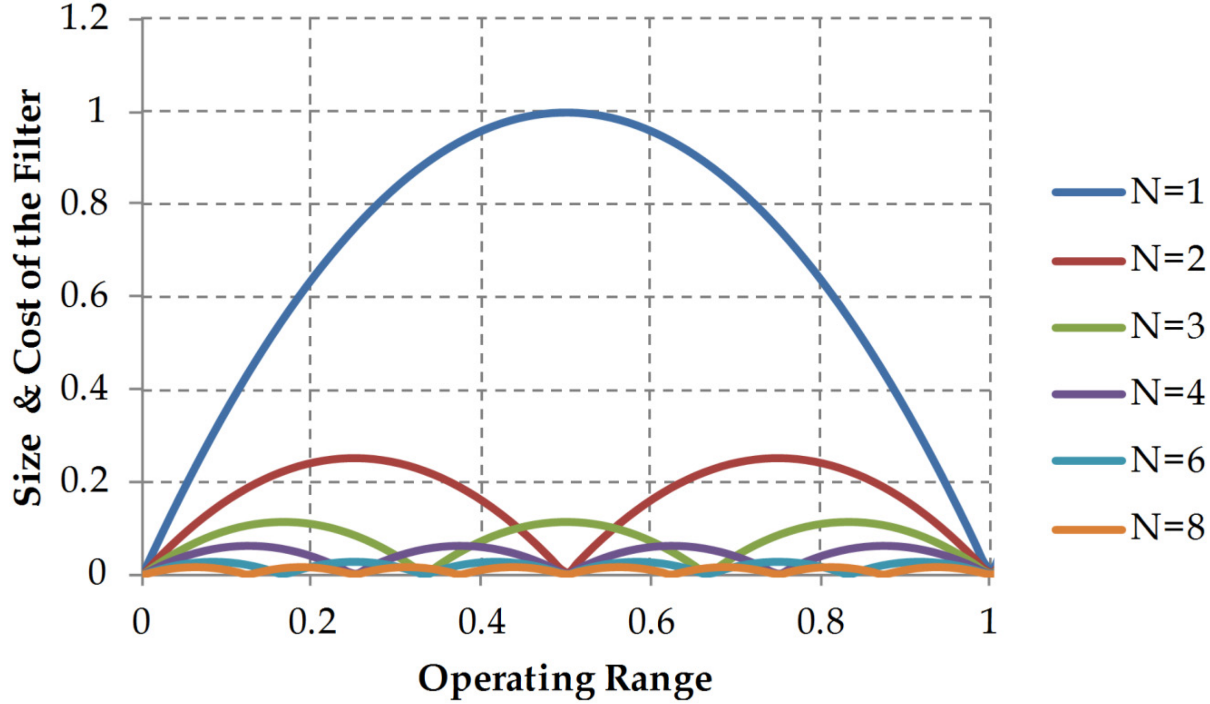
- Input Capacitor & Current Stress!!
- N-Cell Interleaved CSC
  - Small Grid Side Filter Capacitor...
  - Small DC Bus Inductors







Interleaving ➡ Filter cost/size reduction



What ELSE?

Interleaving ⇒ Filter cost/size reduction

What ELSE?

I. Reduced equivalent stray inductance of the switching cell, or

II. Reduced equivalent switching speed of a device

⇒ Higher switching speed is possible

⇒ Better utilization of WBG Devices

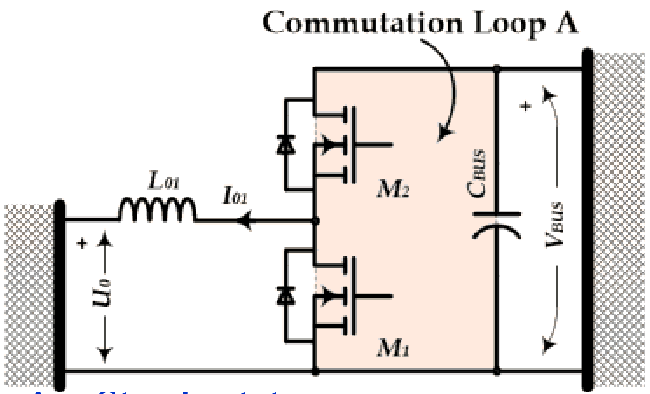
- Particularly case in low voltage high current applications
  - Even today with Si MOSFETs
  - In near future much more with WBG, particularly GaN

Multi-Cell Converters

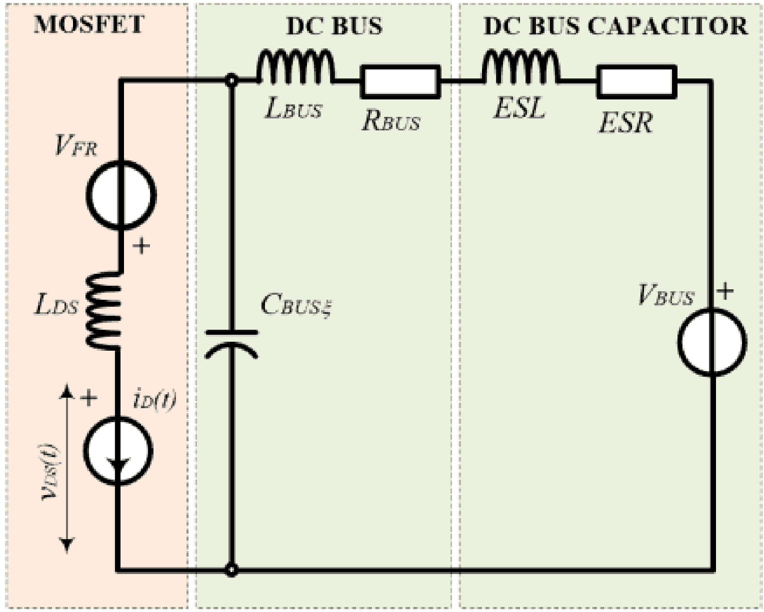
-Synergy with new Power Semiconductors-

...Multi-Cell Converters...

A Basic switching Cell



⇒



An Equivalent Model

A. Steady state
   1. Dc bus voltage,
B. Transient Over-voltage
   2. Total Commutation inductance,
   3. Commutation di/dt,
   4. Number of Cells N
   5. Forward recover voltage,
   6. Effect of resonance

$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

The Switch Total Voltage

...Multi-Cell Converters...

3. The Commutation Inductance L_ξ

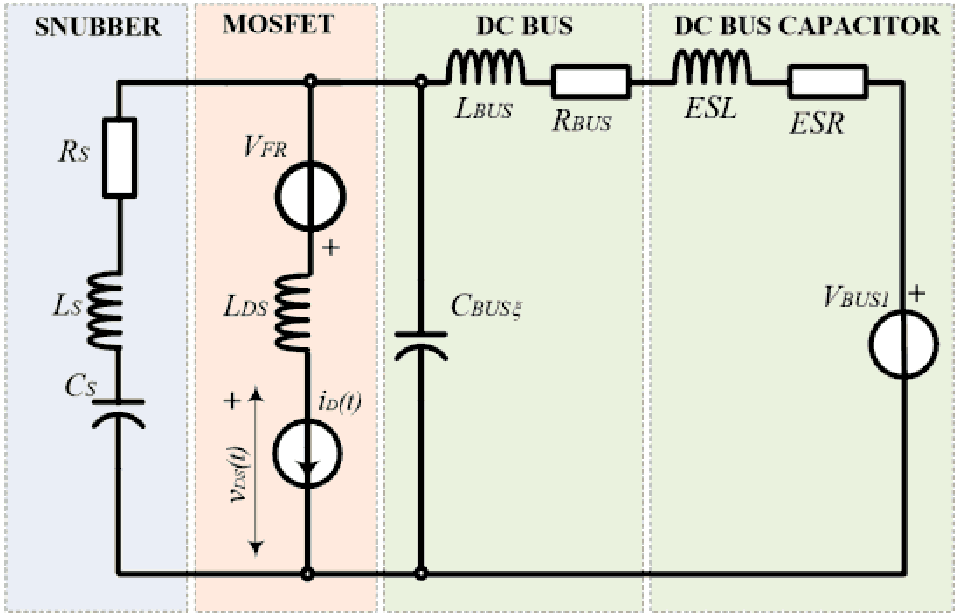
a. The DC Bus Capacitors *ESL*
   - ❑ Low Voltage MLCCC,
     - ❑ 1-10nH

b. The DC Bus Inductance L_{BUS}

Depends on the Current Rating
   - ❑ PCB, 1-5nH
   - ❑ Laminated BUS Bar

c. The Switch Inductance L_{DS}

Depends on the package
   - ❑ Total 10-20nH
   - ❑ OptiMOS <10nH



In Total

I. Theoretically: L_ξ <5nH ☺
...BUT???

II. In Reality: L_ξ >20nH ☹

$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N}\frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

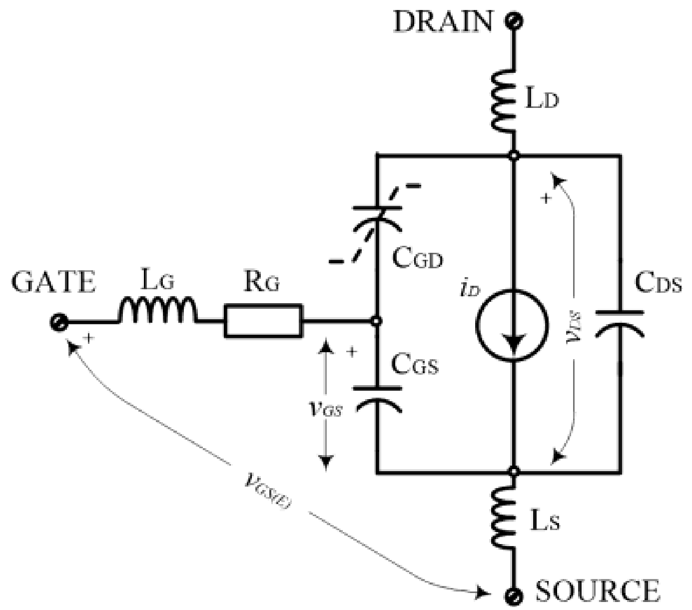
The Switch Total Voltage

...Multi-Cell Converters...

4. The Switch *di/dt*

Simplified linear model

$$\frac{di_D}{dt} = \frac{\frac{I_0}{g_m} + V_{GS(TH)} + |V_{EE}|}{\frac{R_G C_{ISS}}{g_m} + L_S} = k_0 + k_1 I_0 + k_2 |V_{EE}|$$



- Typically

$$R_G C_{GS} << g_m L_S$$

  - R_G neglected ⇒ di/dt is determined by the source inductance L_S
    - di/dt <2kA/µs ⇒ t_F>100ns @200A
      - *Losses ??*

$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

The Switch Total Voltage

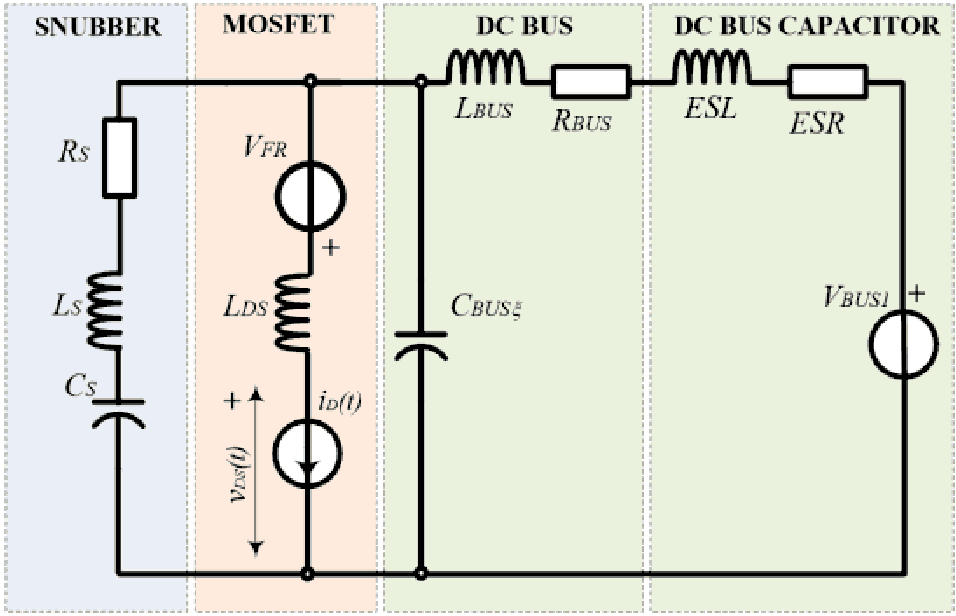
Controllability (and Losses reduction !!)

A. Separate the power and control source

B. Negative gate-source voltage V_{EE}

5. **FWD Forward Recovery Voltage**
   - The FWD initial resistance can be high,
   - Overshoot, may go up to 30V

6. **Effect of Resonance**
   - Resonance of the dc bus can amplify to over-voltage
     - $k_R > 1$

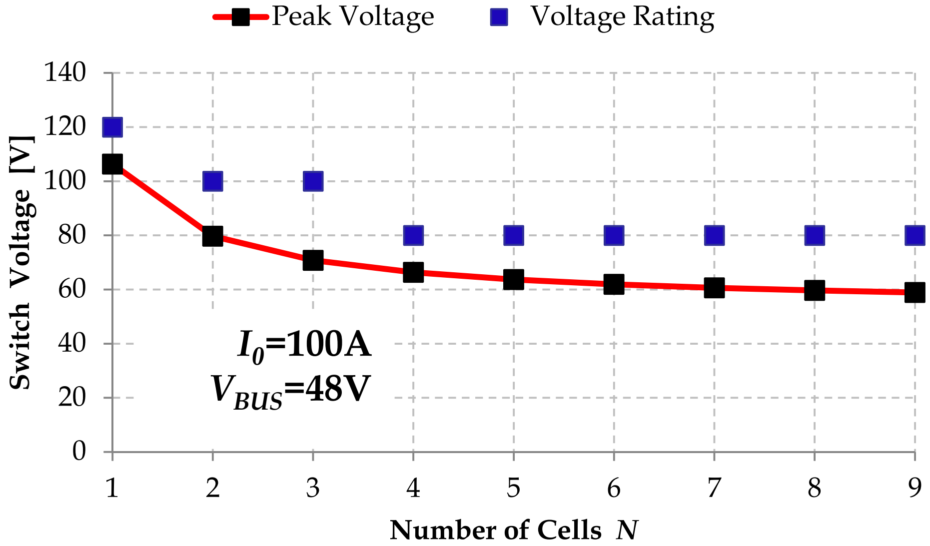


$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

The Switch Total Voltage

...Multi-Cell Converters...

$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt}}_{TRANSIENT} + V_{FR}$$

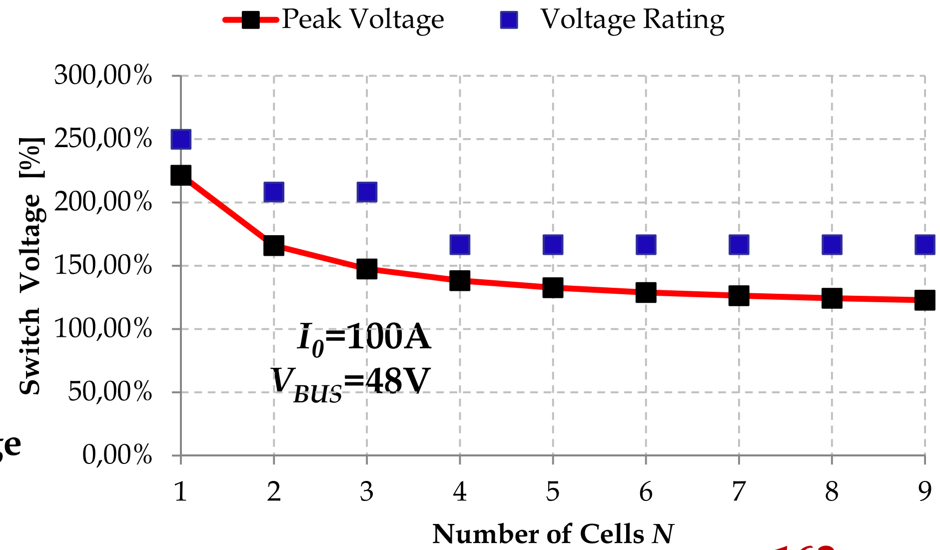


Equivalent commutation inductance is reduced with number of cells N

- ❖ **Only way to go beyond the limit of Si**
- ❖ **and ...use full benefit of WBG...**

$$\frac{V_{DS}}{V_{BUS}} = 1 + \left[\underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt}}_{TRANSIENT} + V_{FR} \right] \frac{1}{V_{BUS}}$$

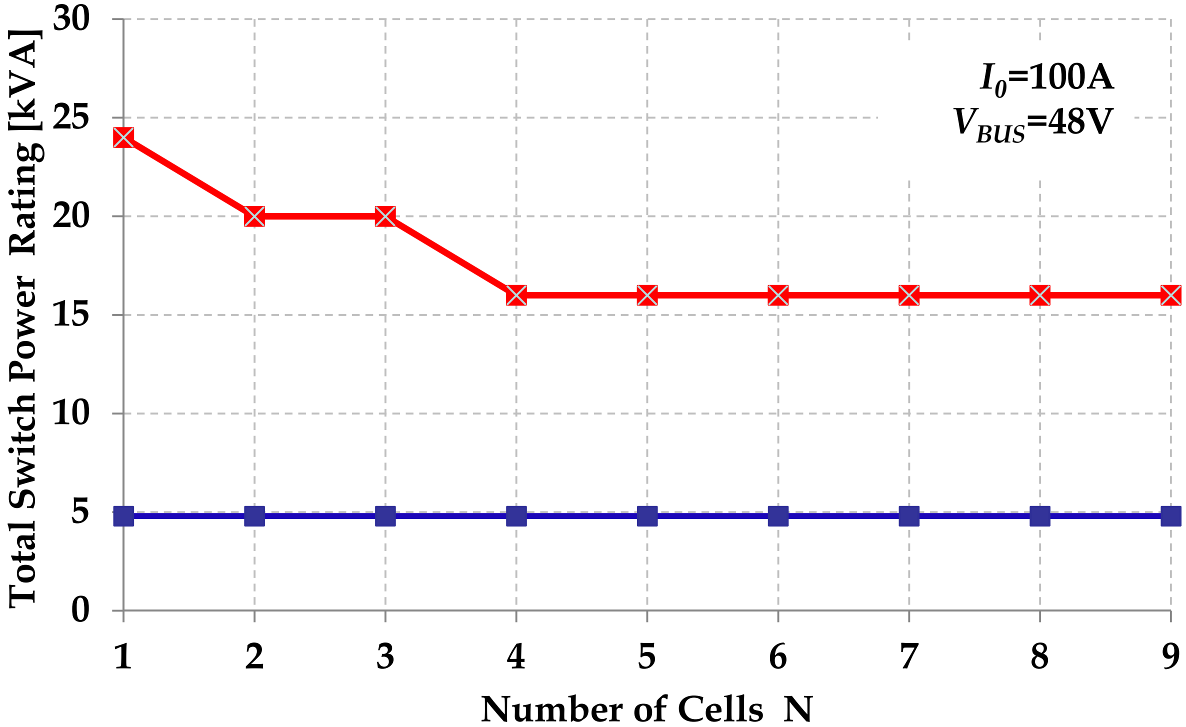
The Switch Relative (Normalized) Voltage



...Multi-Cell Converters…

Total Power of all Semiconductors Switch

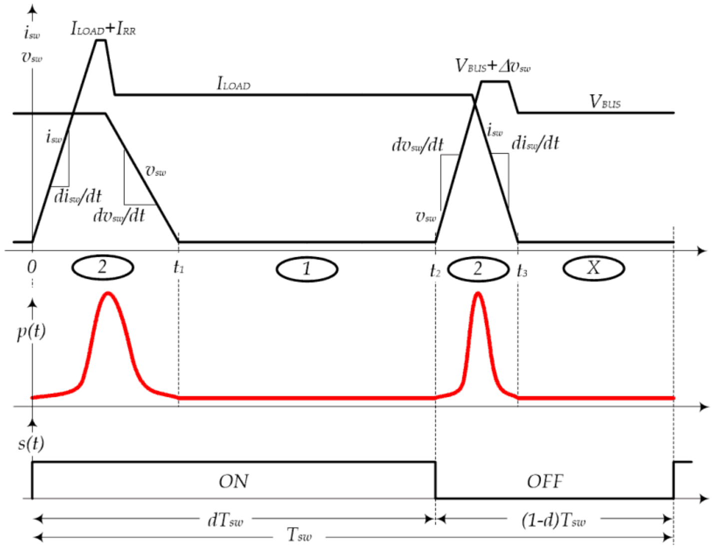
$$\sum_{1}^{N_{SW}} S_{(j)} = SN_{SW} = 2\left(V_{BUS} + k_R L_\zeta \frac{1}{N}\frac{di_D}{dt} + V_{FR}\right) I_0$$



...Multi-Cell Converters…

1. **Conduction Losses**

$$P_{CON} = \frac{I_0^2}{N} R_{DS(N)}$$



2. **The Switch Commutation Losses**
   i. Voltage/Current overleaping
   ii. Parasitic Inductance Energy
   iii. Parasitic Capacitance Energy

$$P_{SW} \cong \left\{ \underbrace{V_{BUS} I_0 \frac{(t_{iF} + t_{vR} + t_{iR} + t_{vF})}{2}}_{i} + \underbrace{\frac{1}{2} L_\zeta}_{ii} \frac{I_0^2}{N} + \underbrace{N \frac{1}{2} V_{BUS}^2 C_{OSS}}_{iii} \right\} f_{SW}$$

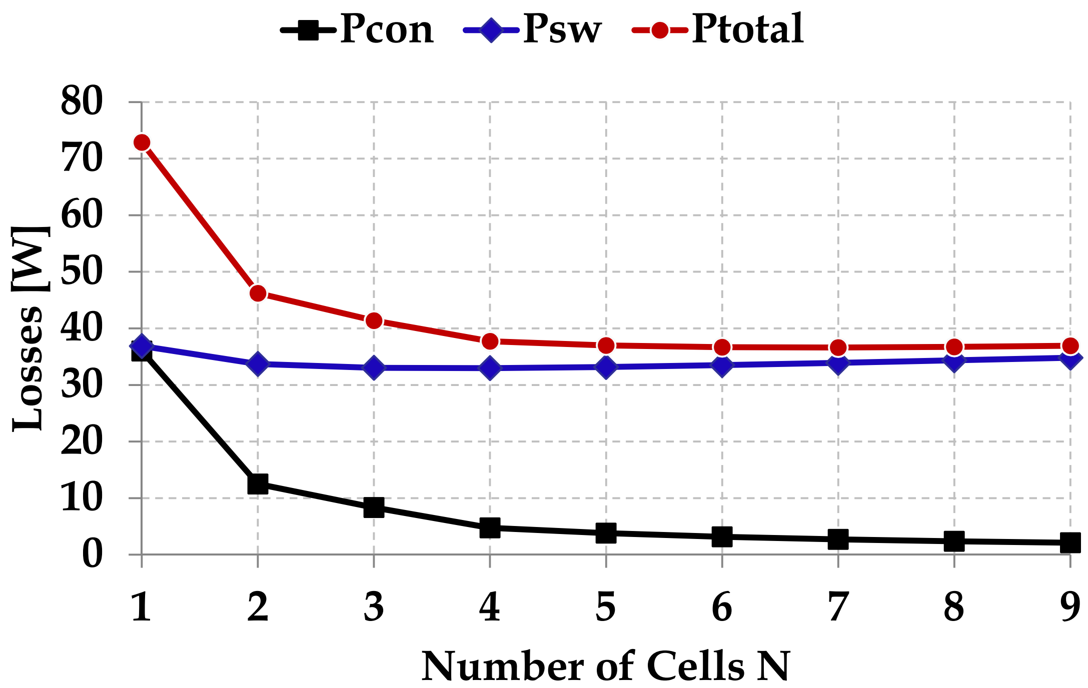
3. **The FWD Commutation Losses**

$$P_D \cong \left\{ V_{BUS} I_0 \frac{E_Q}{U_N I_N} \right\} f_{SW}$$

...Multi-Cell Converters...

- f_{SW} =Constant
- Δi_0= Constant

  Size (Cost) of the Filter
  ↓↓



$$L_0 = \frac{V_{BUS}}{f_{SW} N 4 \Delta i_{0\,max}}$$

MOSFET losses versus number of levels *N*.

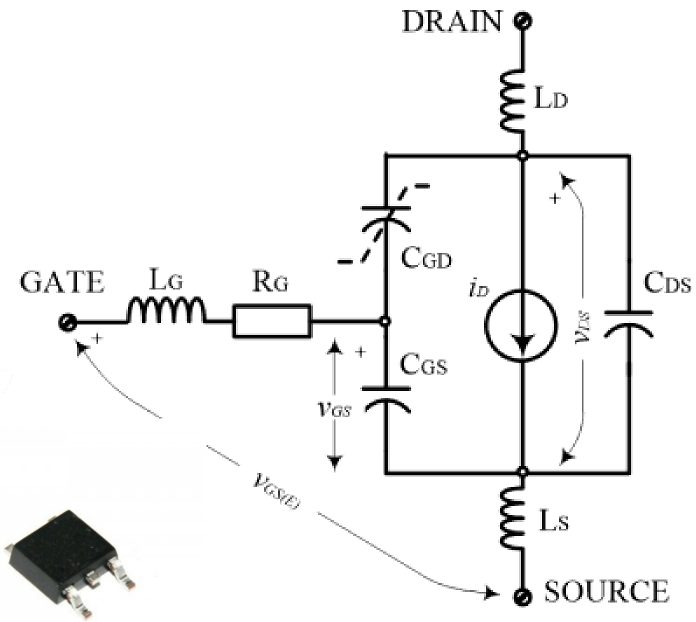
- The dc bus voltage V_{BUS}=48V,
- The load current I_0=100A,
- The switching frequency is constant f_{SW}=100kHz.

...Multi-Cell Converters…

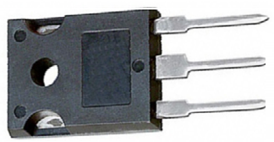
GaN MOSFET

Simplified linear model

$$\frac{di_D}{dt} = \frac{\frac{I_0}{g_m} + V_{GS(TH)} + \left|V_{EE}\right|}{\frac{R_G C_{ISS}}{g_m} + \frac{L_S}{N}} = k_0 + k_1 I_0 + k_2\left|V_{EE}\right|$$



- $V_{GS(TH)}$=1-2V
- TO247 or TO220 Package
  - di/dt <0.5kA/µs ⇒ t_F>400ns @200A
- Even TO 252 and similar package makes no big difference



What is The Solution

I. Reduce the Inductance *Ls*
   - Lead-less package is MUST

II. Reduced current per a chip
   - Interleaving

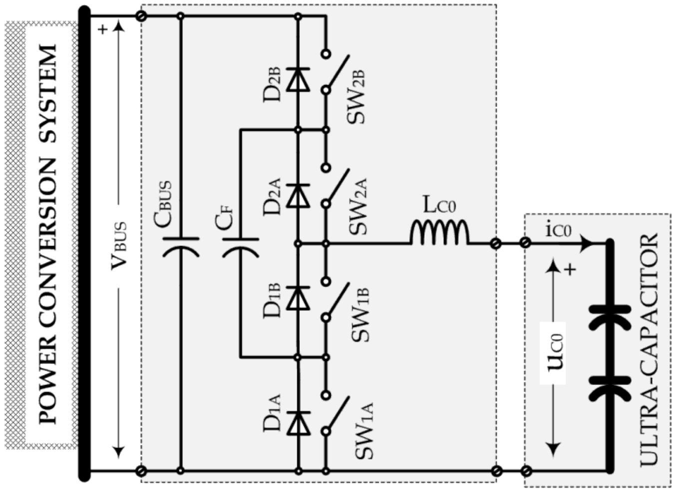
III. Negative gate-source voltage V_{EE}

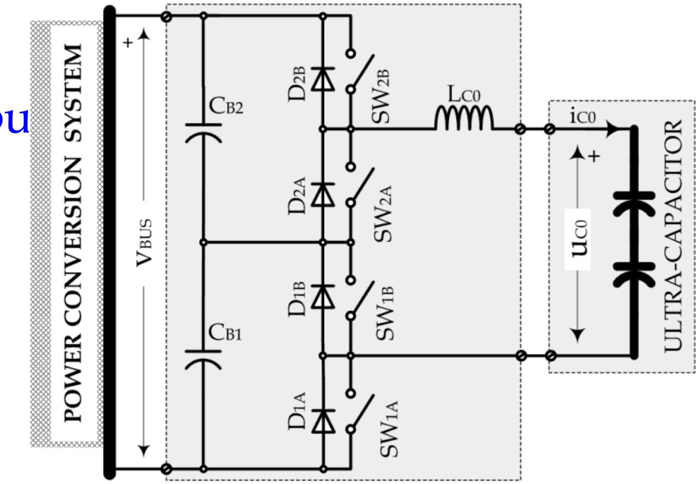
Multi-Level Converters

Multi level converters

- The device voltage rating, $V_{BUS}/(n-1)$
    - Cost effective , high efficiency
- Small output filter inductor
- Small input filter capacitor
- Complex control
- The voltage gain $m \leq 1$

3. Three-level flying capacitor convertor
    - The ultra-capacitor reference is minus dc bu
    - An additional flaying capacitor
4. Three-level flying output convertor
    - No additional components
    - The ultra-capacitor is floating, Common mode voltage





Multi-level Converters

-Split the input voltage into segments-

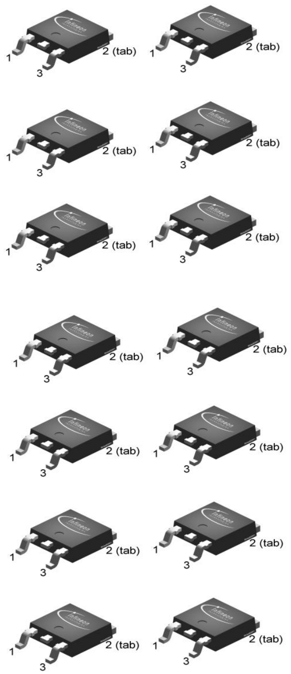
Why we need to split the input (dc bus) voltage into segments?

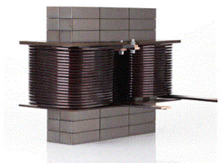
I. Good topic for (university) research,
II. Can we do something for passives (Inductors & Capacitors)?
III. Something else?
IV. And, is it a logical step?

...Multi-level Converters...

We need an Inductor-free converter…

- ❑ No additional inductors or just very small one..parasitic stray inductance…



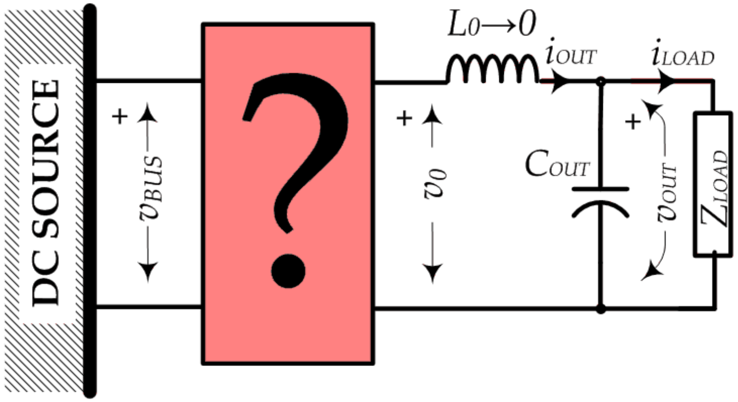


...Multi-level Converters...

- An Inductor-free converter…no additional inductors or just very small one..parasitic stray inductance…
- The Inductance is proportional to flux
  - And the flux is volt-second on the inductor

$$L \approx \psi = \Delta v_{L0} \Delta T \approx \frac{\Delta v_0}{f_{SW}} k_{op}$$

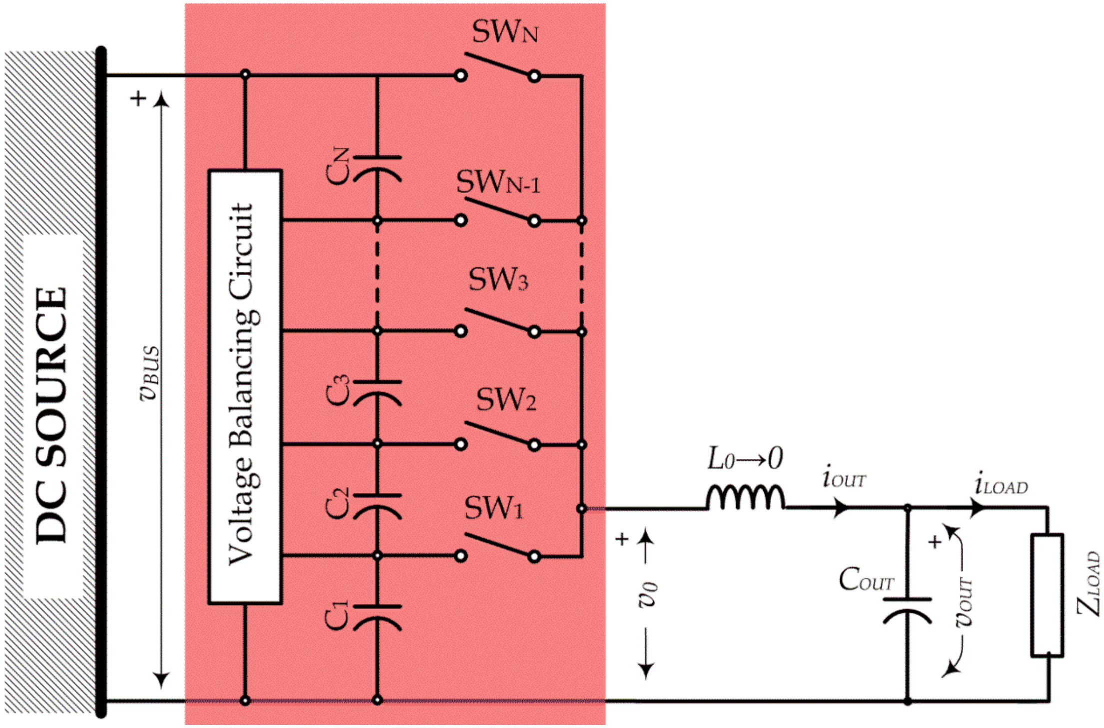
A. Increase switching frequency f_{SW},
   - Nice, but not for free…switching l
B. Reduce voltage step Δv_0,
   - Also nice, but how?
C. Or, can we play on k_{op}?
   - It looks possible, but how?



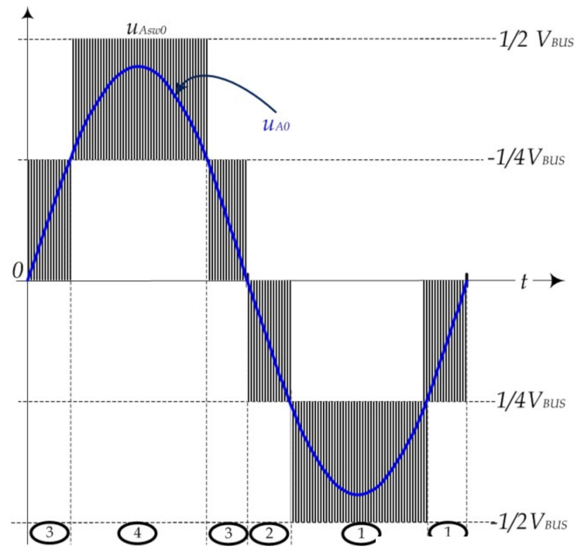
...Multi-level Converters...

- Instead of full dc bus voltage v_{BUS} on the filter
- We may apply the voltage in small steps
  - Multi-level power converters

$$L \approx \psi = \Delta v_{L0} \Delta T \approx \frac{\Delta v_0}{f_{SW}} k_{op}$$



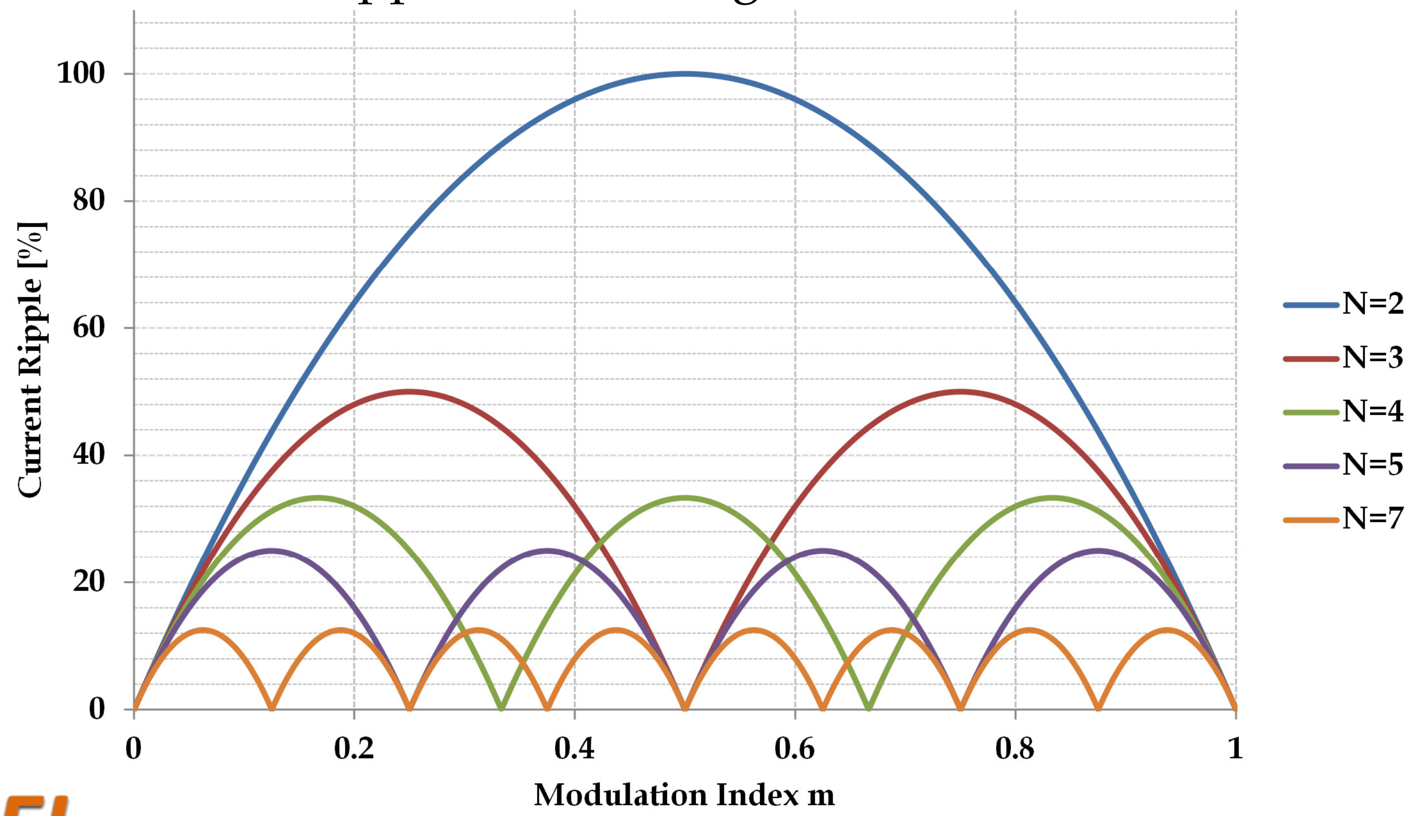
$$\Delta i_0 = \frac{V_{BUS}}{f_{SW} L_0 (N-1)} (d^2 - d)$$



...Multi-level Converters...

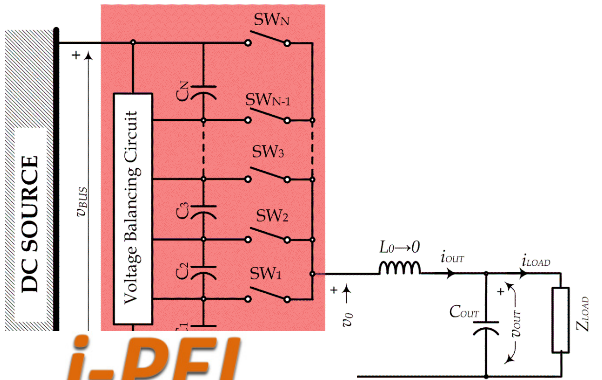
$$\Delta i_0 = \frac{V_{BUS}}{f_{SW} L_0 (N-1)} \left[\left((N-1)m - floor((N-1)m) \right) - \left((N-1)m - floor((N-1)m) \right)^2 \right]$$

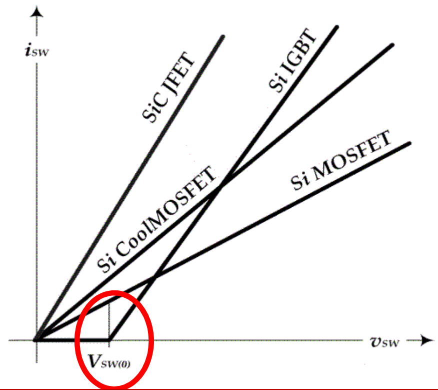
Current ripple overall range of modulation index m

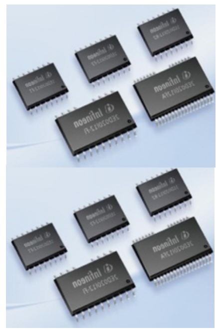


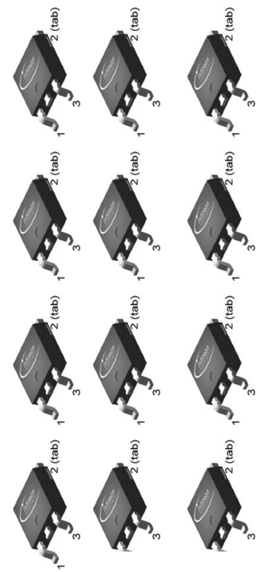
...Multi-level Converters...

- Multi-level power converters are state of the art in high voltage high power applications
  - Not yet case in low voltage low power application
- What device ? Bipolar (IGBT) or Unipolar (MOSFET)?
- Low voltage Unipolar devices are preferred
  - CoolMOS, OptiMOS
- But, what topology?
- How to control such a complex converter?

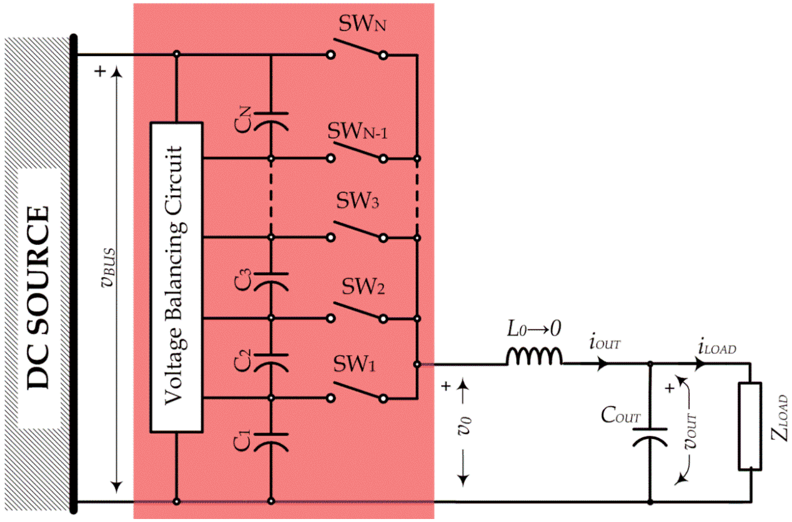


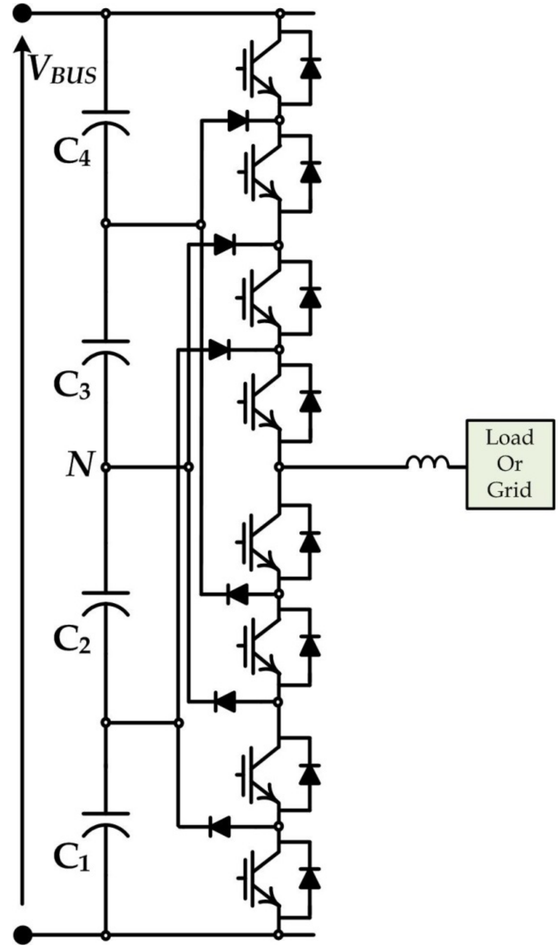


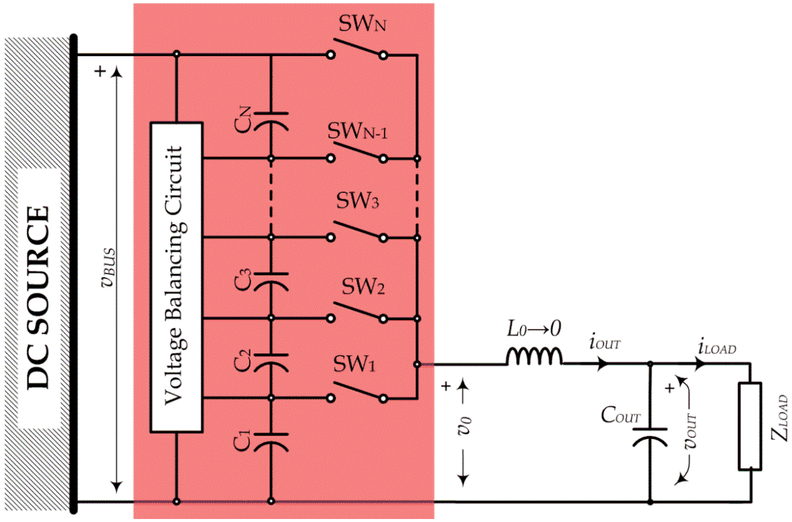




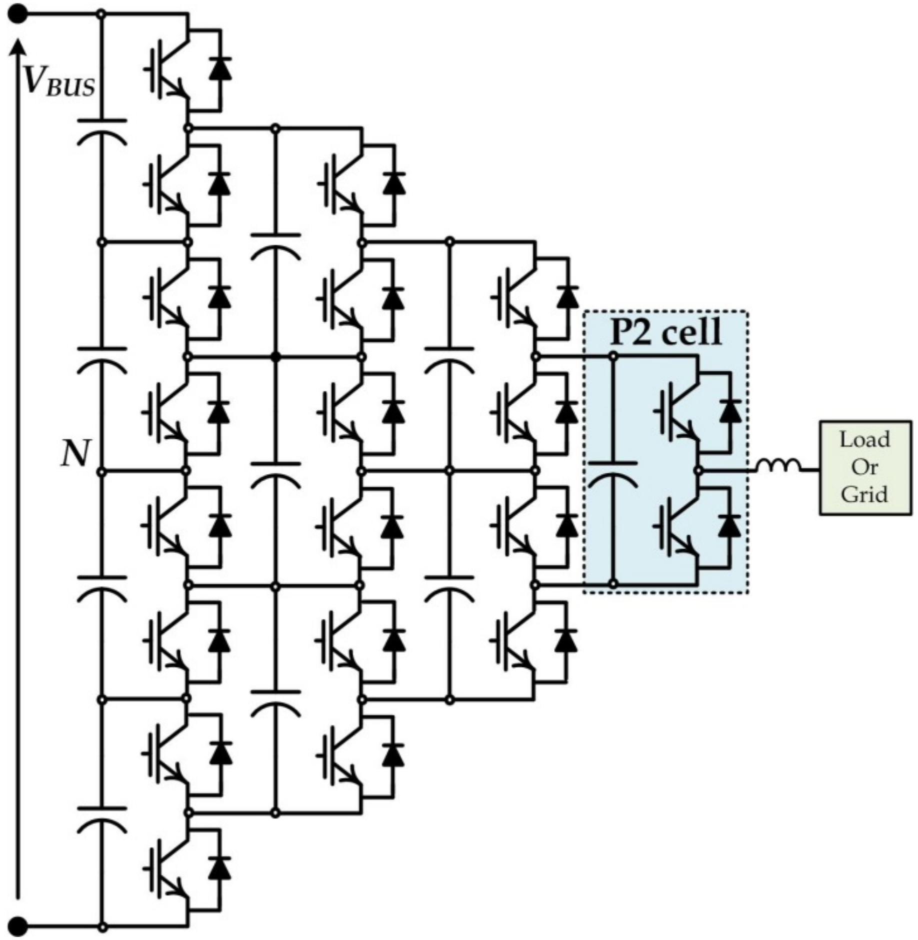
...Multi-level Converters...





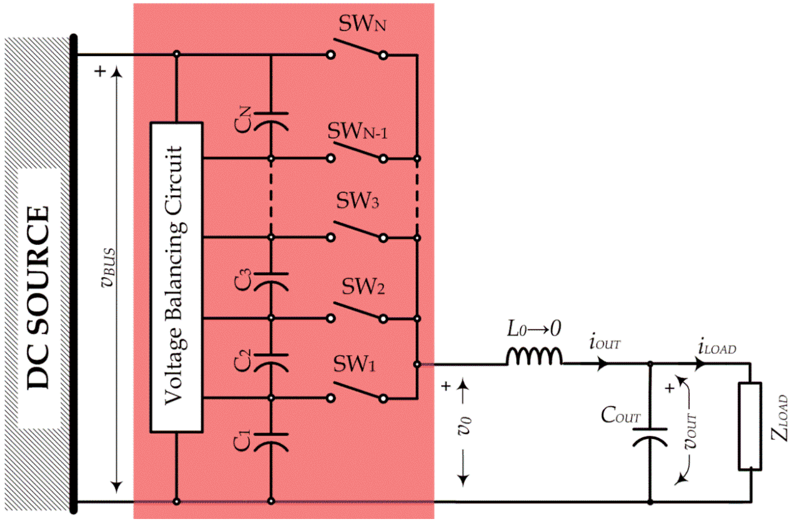


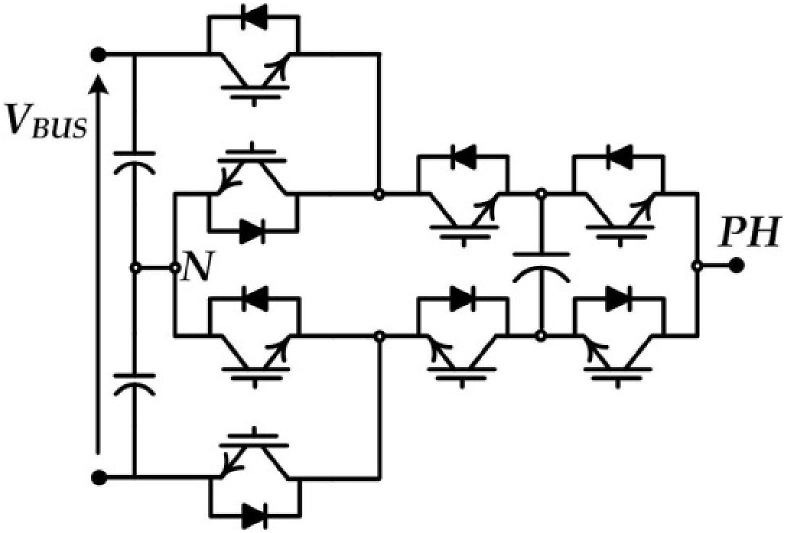
DC SOURCE
v_{BUS}
Voltage Balancing Circuit
SW_N
SW_{N-1}
SW_3
SW_2
SW_1
C_N
C_3
C_2
C_1
$L_0 \rightarrow 0$
i_{OUT}
i_{LOAD}
v_0
C_{OUT}
v_{OUT}
Z_{LOAD}



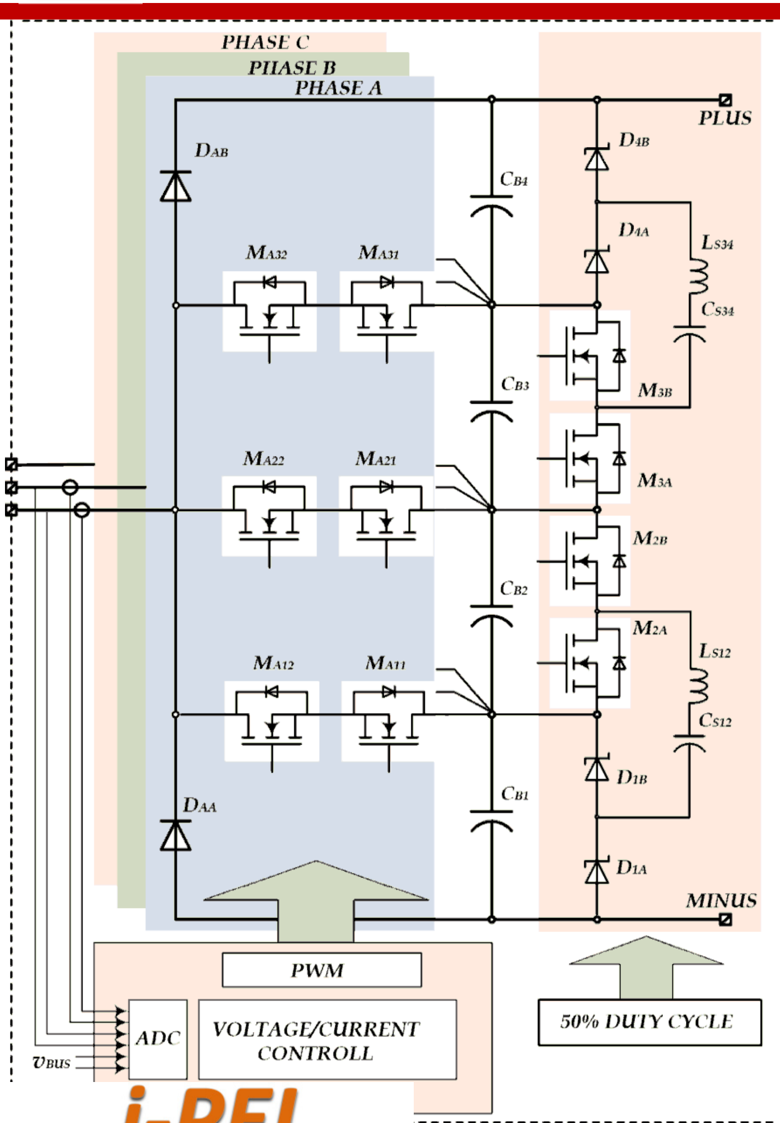
V_{BUS}
N
P2 cell
Load
Or
Grid

...Multi-level Converters...

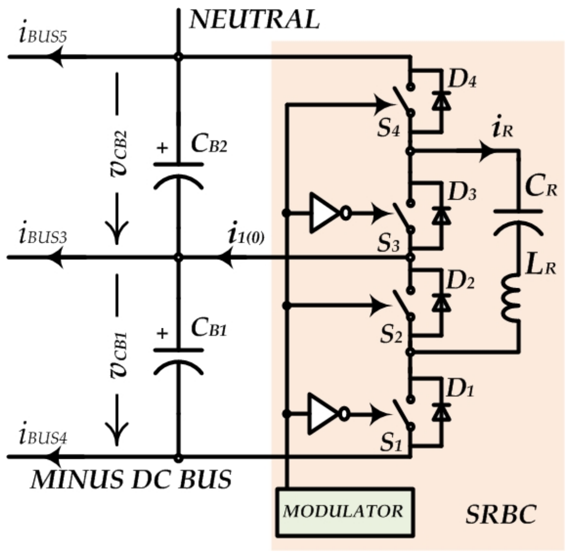




...Multi-level Converters...

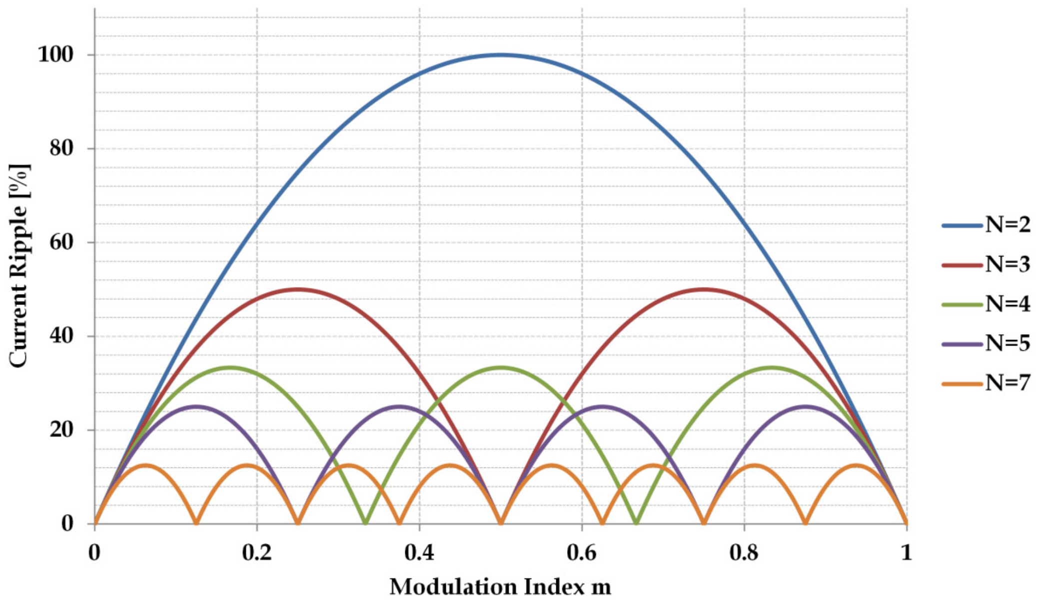


P. J. Grbović, F. Crescimbini, A. Lidozzi and L. Solero, "5-Level Unidirectional T-Rectifier for High Speed Gen-Set Applications," ECCE America 2014, Pittsburg, USA, 14-18 September, 2014.



...Multi-level Converters...

Multi-level ➡ Filter cost/size reduction



What ELSE?

- What about the load voltage and the load stress?

C_P-The load parasitic capacitance

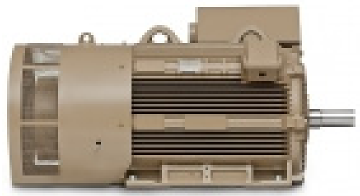
$$i_{CP} = C_P \frac{du_{LOAD}}{dt}$$

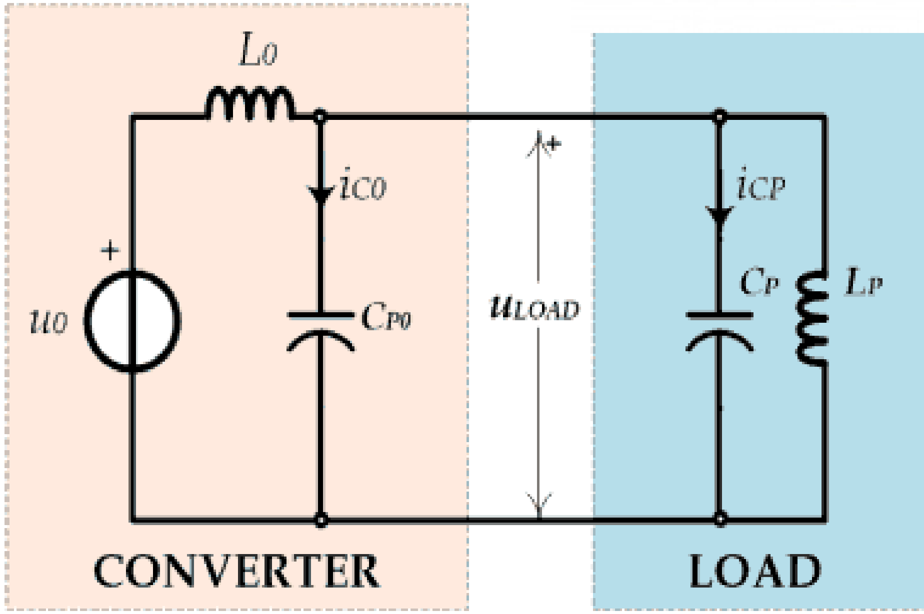
- Just an indication,
- Much more complex in the reality,

I. $dE/dt \approx dv/dt$ is critical for the load insulation
   - *dv/dt should be <10kV/µs*

II. Voltage reflection

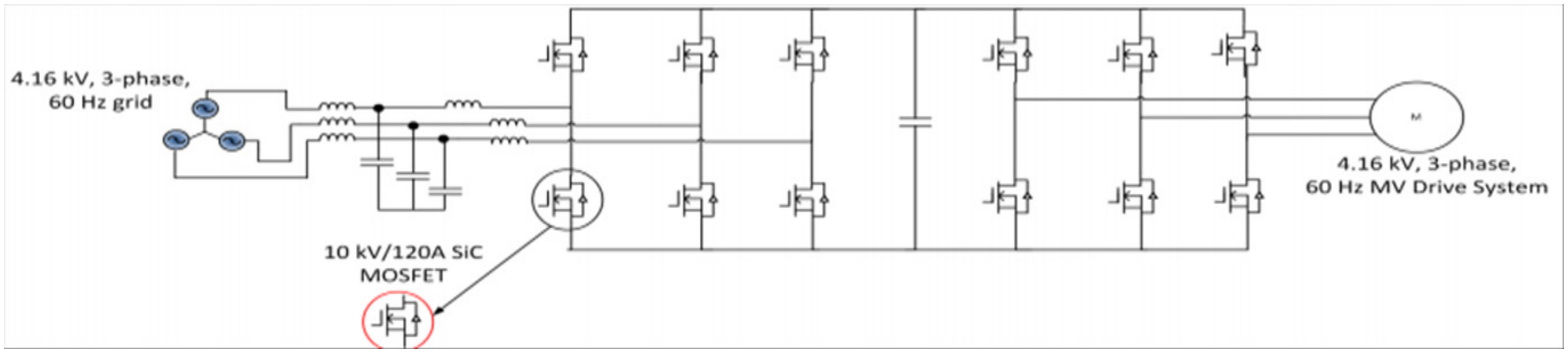
III. The machine shaft parasitic current





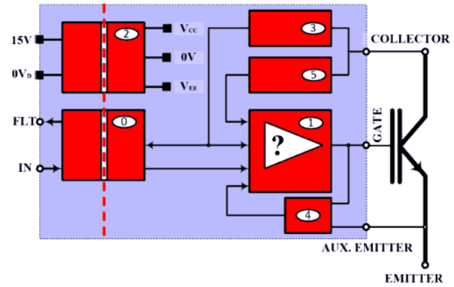
...Multi-level Converters...

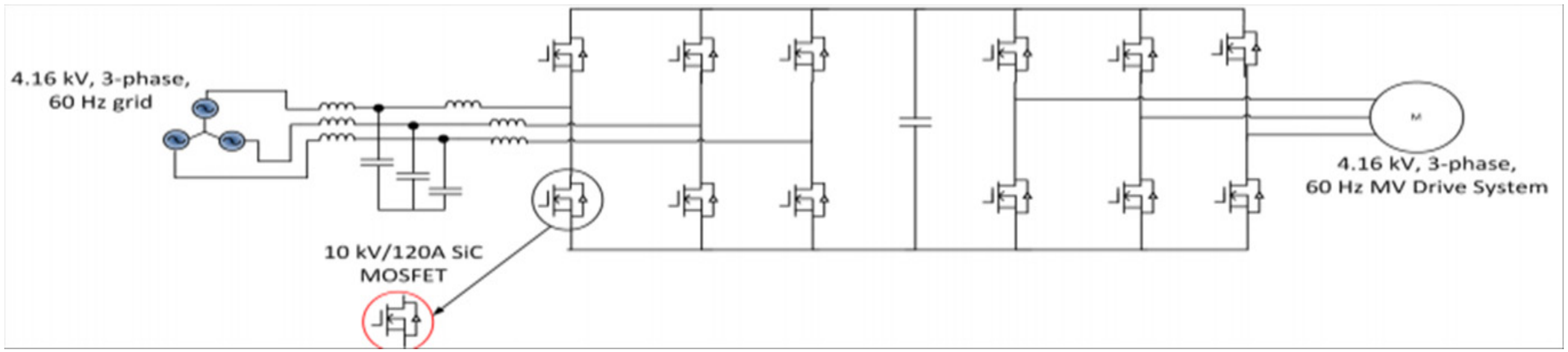
- **In General, electrical machines do not like** **high *dv/dt*** **stress**
- **BUT, what we are doing is completely opposite!!**
- A new WBG (SiC MOSFET) switch **10kV&120A @ 100-200ns**
  - *35-70kV/μs*



...Multi-level Converters...

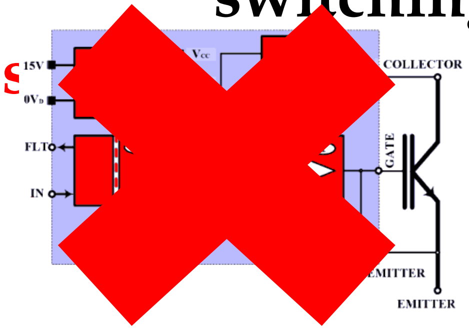
- Can we use an active gate driver and slowdown the switching?

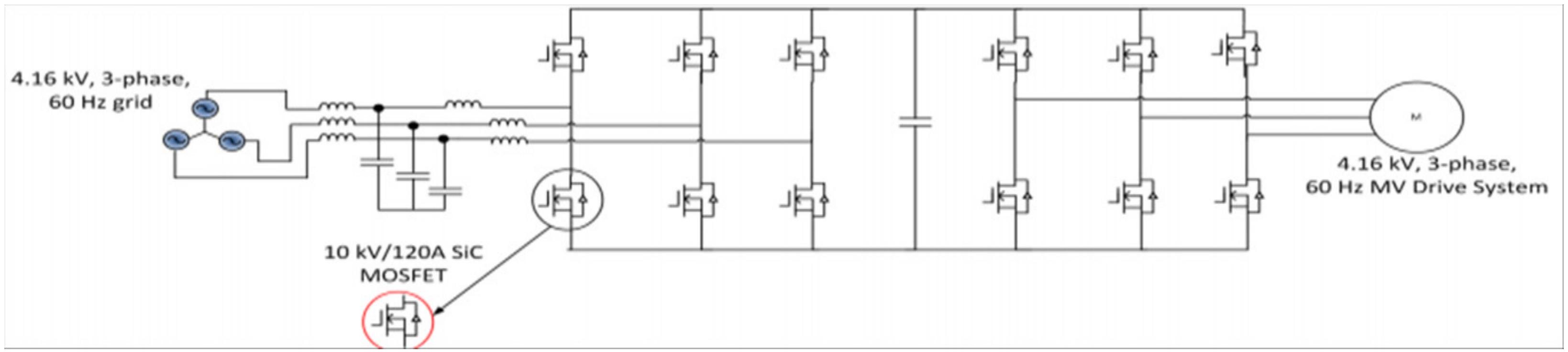




...Multi-level Converters...

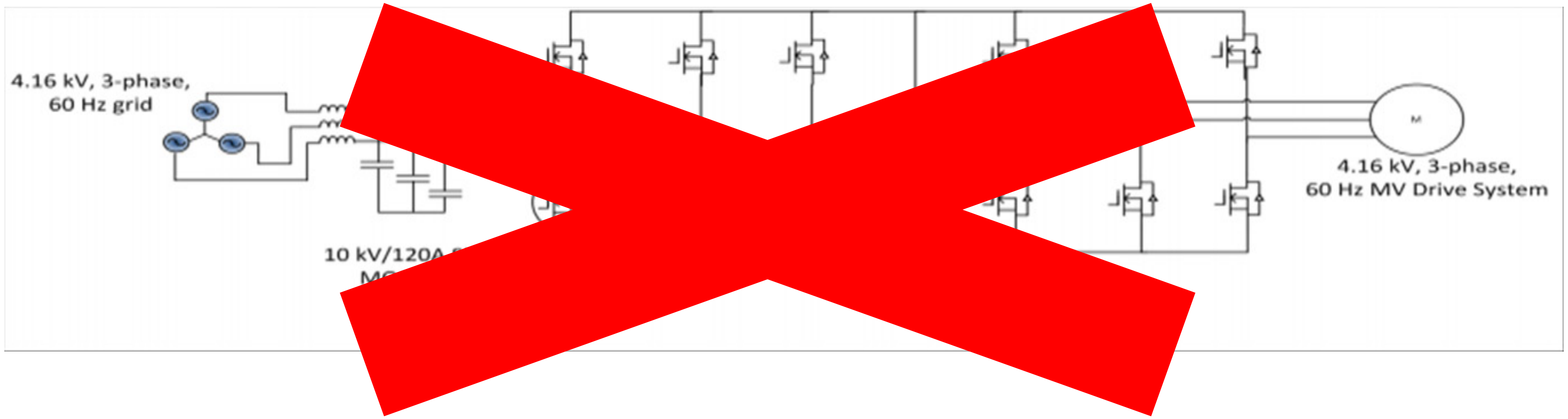
- Can we use an active gate driver and slowdown the switching?
  - Yes, but it does ... e!!





...Multi-level Converters...

- Can we use an active gate driver and slowdown the switching?
- Yes, but it does not make sense!!
- We Must split the dc bus voltage into segments and apply segment by segment on the load
  - Multi-level switching not 2-level switching



What about low-voltage high-current conversion?

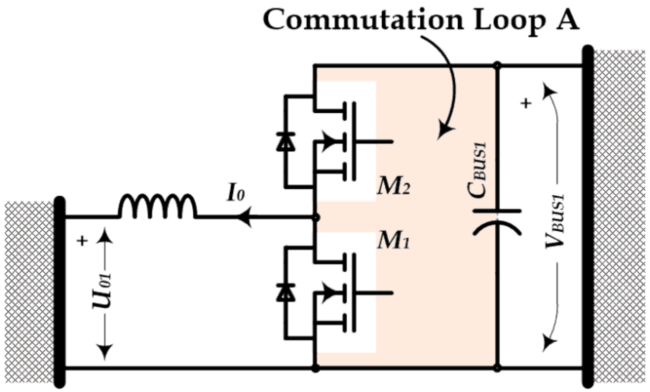
3) Switch(s) Voltage Rating
   - Select proper devices with proper voltage rating

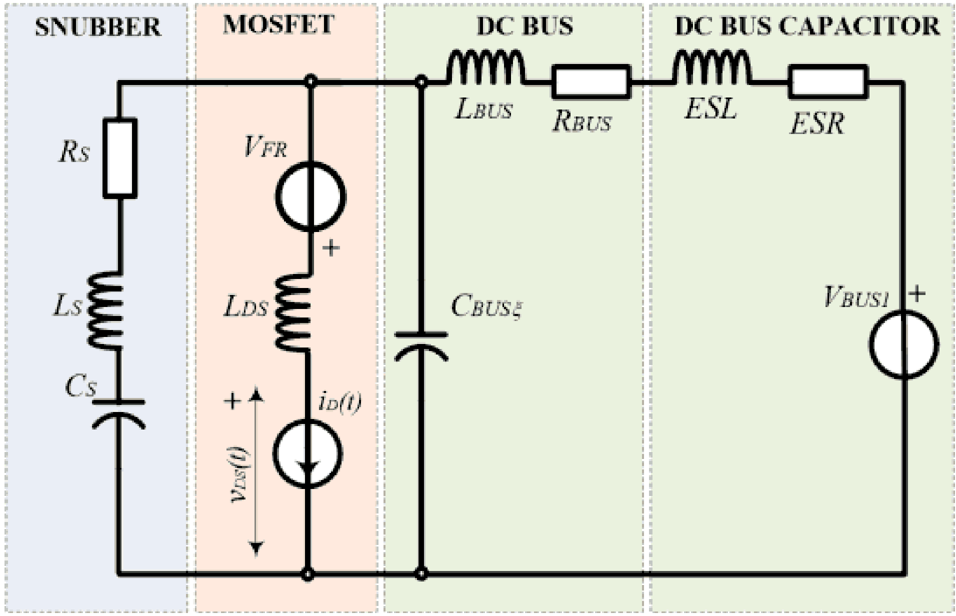
4) Switch(s) (Total) Power Rating
   - What is total power of Semiconductors?
   - Is it optimal or not?
   - $N=x$ or $N=y$, which one is better

5) Conversion Losses
   - Optimization: efficiency, size and cost?
   - $N=x$ or $N=y$, which one is better

...Multi-level Converters...

A Basic switching Cell





Small Signal Model

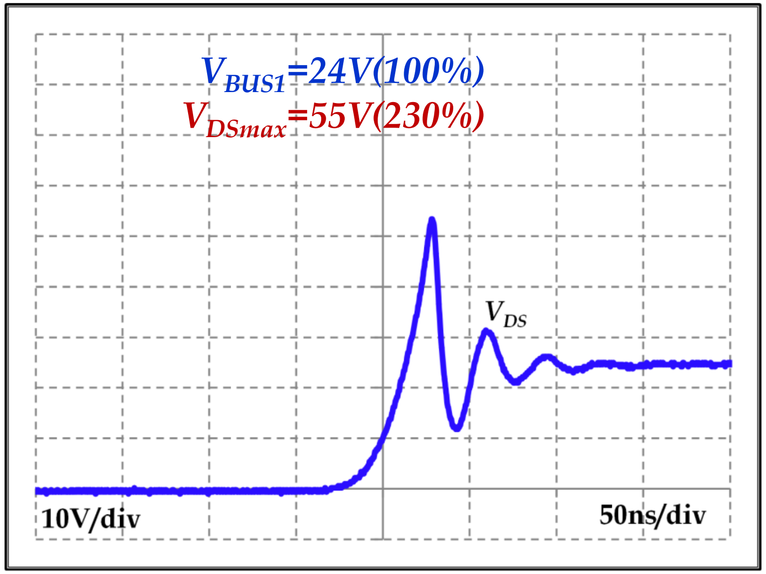
The Switch Voltage Rating

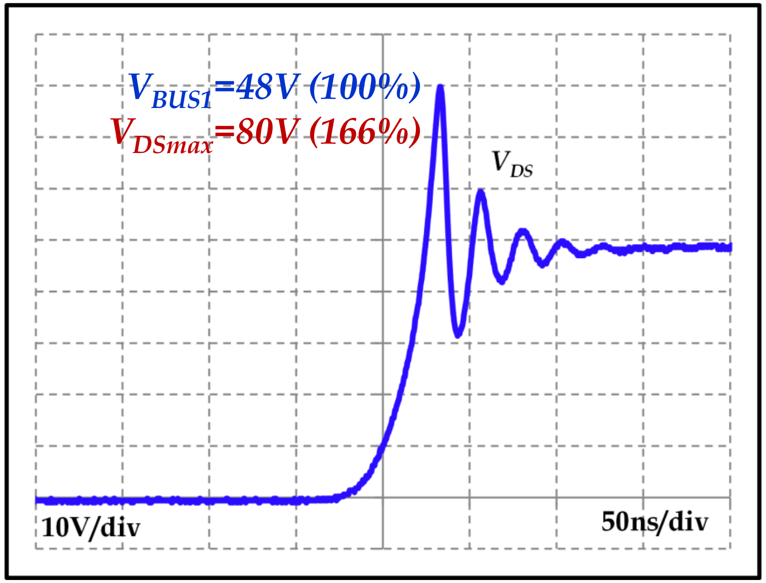
A. Steady state
   1. Dc bus voltage,
   2. Number of Levels

B. Transient Over-voltage
   3. Total Commutation inductance,
   4. Commutation di/dt,
   5. Forward recover voltage,
   6. Effect of resonance

$$V_{DS} = \frac{V_{BUS}}{(N-1)} + \underbrace{k_R L_\zeta \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

The Switch Total Voltage





Experimental waveforms of drain source turn-off voltage v_{DS}

- **The cell dc bus voltage V_{BUS1}=24V (left) and V_{BUS1}=48V (right).**
- **OptiMOS PB019N08**
- **Load current I_0=150A**
- **Gate resistance R_G=1Ω,**
- **Gate driver off state voltage V_{EE}=-5V**

...Multi-level Converters...

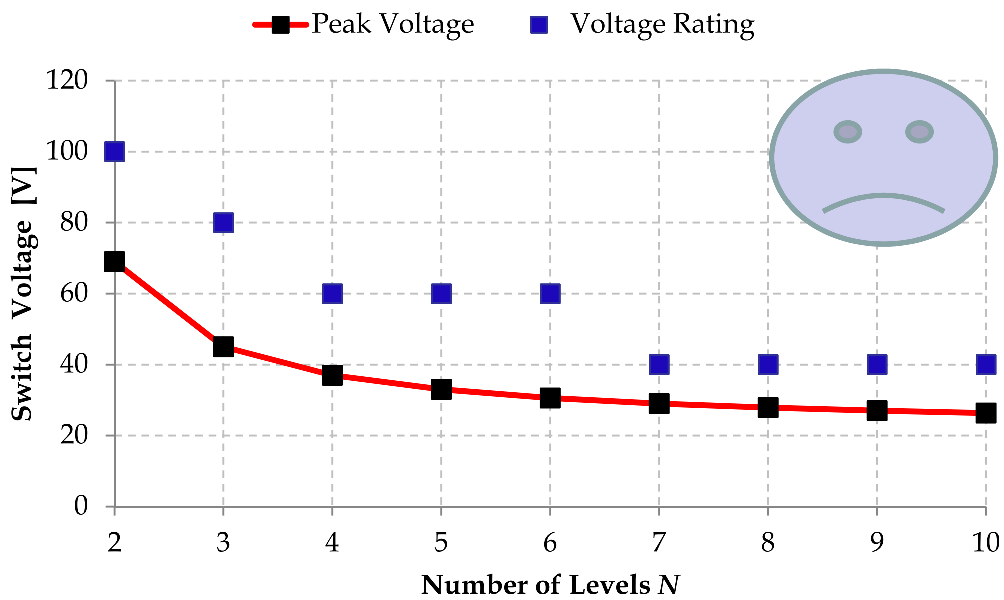
	V_{DS} [V]	R_{DS} [mΩ]	G_m [S]	t_F [ns]	t_R [ns]	C_{ISS} [nF]	C_{OSS} nF]
Maximum Drain Current I_D=180A			Source Inductance L_S=5nH			Forward Recovery Voltage V_{FR}=5V	
IPB009N03	30	0.95	370	26	22	20	6
IPB011N04	40	1.1	370	25	21	22	4.1
IPB016N06	60	1.6	245	35	38	21	3.3
IPB019N08	80	1.9	206	28	33	11	2.9
IPB025N10	100	2.5	200	34	28	11	2
IPB036N12	120	3.6	195	25	21	10.5	1.3

Switch peak voltage and the switch rating versus number of levels *N*.

- V_{BUS}=48V
- I_0=100A

N>6, the voltage rating constant!

- **Defined by the over-voltage not the number of levels N**



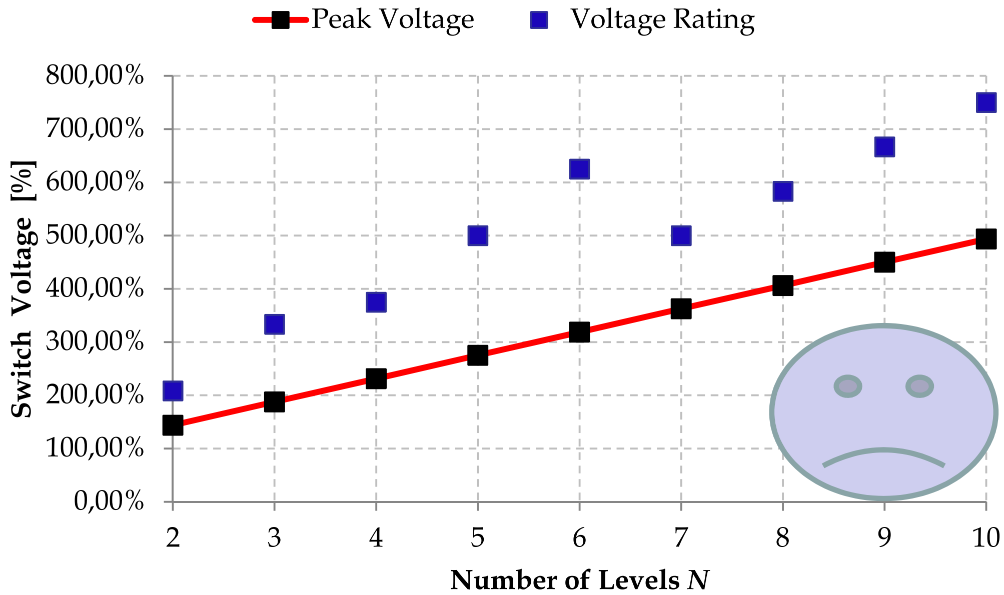
...Multi-level Converters...

	V_{DS} [V]	R_{DS} [mΩ]	G_m [S]	t_F [ns]	t_R [ns]	C_{ISS} [nF]	C_{OSS} nF]
Maximum Drain Current I_D=180A			Source Inductance L_S=5nH		Forward Recovery Voltage V_{FR}=5V		
IPB009N03	30	0.95	370	26	22	20	6
IPB011N04	40	1.1	370	25	21	22	4.1
IPB016N06	60	1.6	245	35	38	21	3.3
IPB019N08	80	1.9	206	28	33	11	2.9
IPB025N10	100	2.5	200	34	28	11	2
IPB036N12	120	3.6	195	25	21	10.5	1.3

The Switch normalized peak voltage =f(*N*).

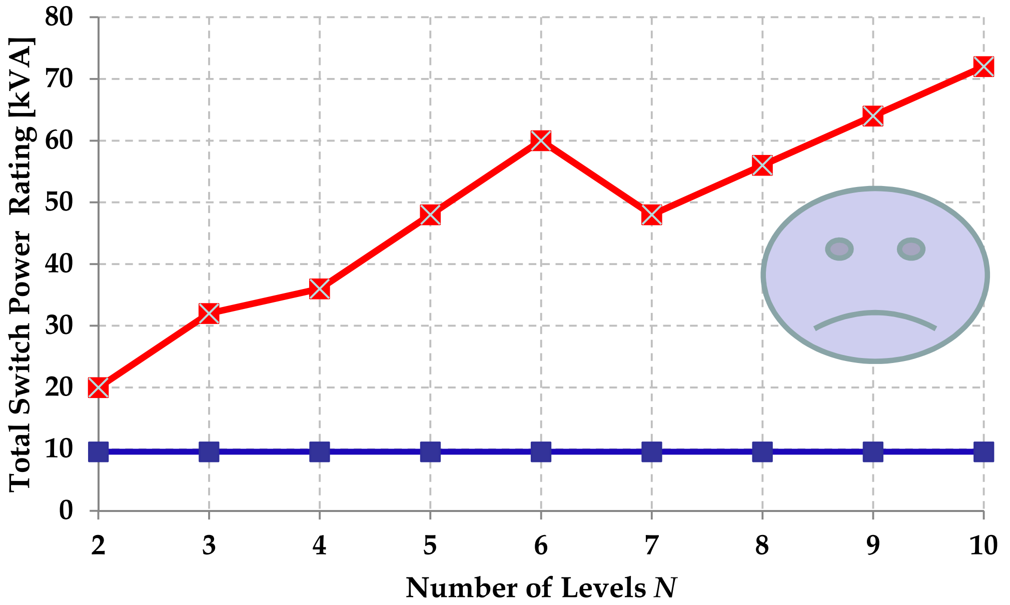
$$\frac{V_{DS}}{\frac{V_{BUS}}{(N-1)}} = 1 + \left[\underbrace{k_R L_\zeta \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}\right]\frac{(N-1)}{V_{BUS}}$$

- V_{BUS}=48V
- I_0=100A



Total Power of all Semiconductors Switch

$$\sum_{1}^{N_{SW}} S_{(j)} = SN_{SW} = 2(N-1)\left(\frac{V_{BUS}}{(N-1)} + k_R L_\zeta \frac{di_D}{dt} + V_{FR}\right) I_0$$



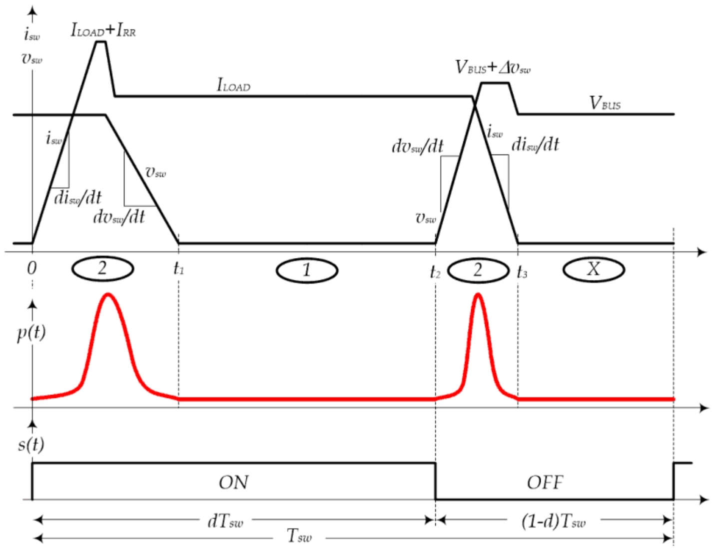
- I_0=100A
- V_{BUS}=48V

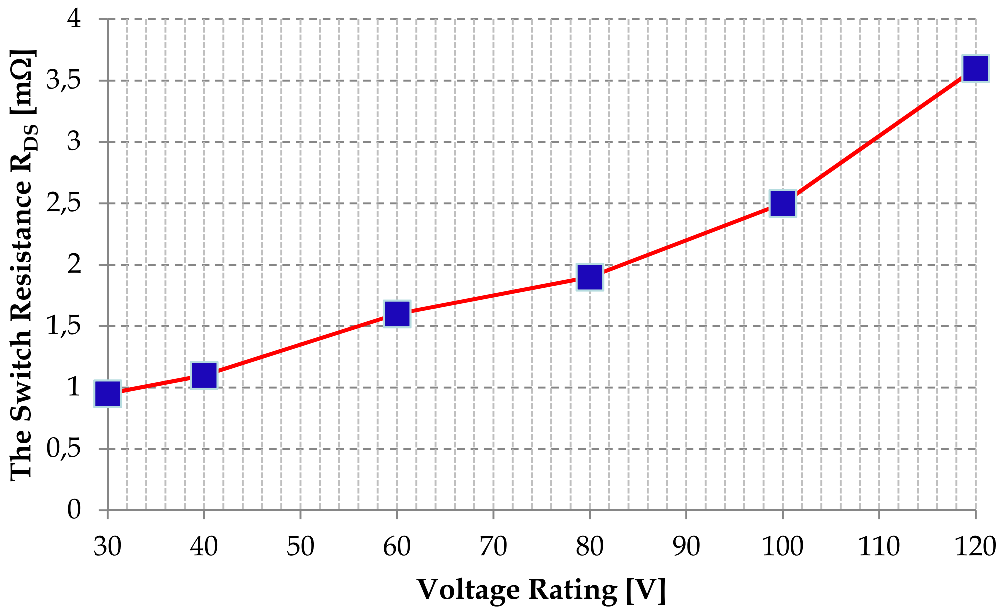
Is this correct?
Not completely, but it gives an indication....

1. Conduction Losses

$$P_{CON} = (N-1) I_0^2 R_{DS(N)}$$

- ❑ **Depend on number of Levels *N***
  - ❑ R_{DS}= *Function* (The blocking voltage)





Low voltage MOSFET resistance R_{DS} versus rated voltage.

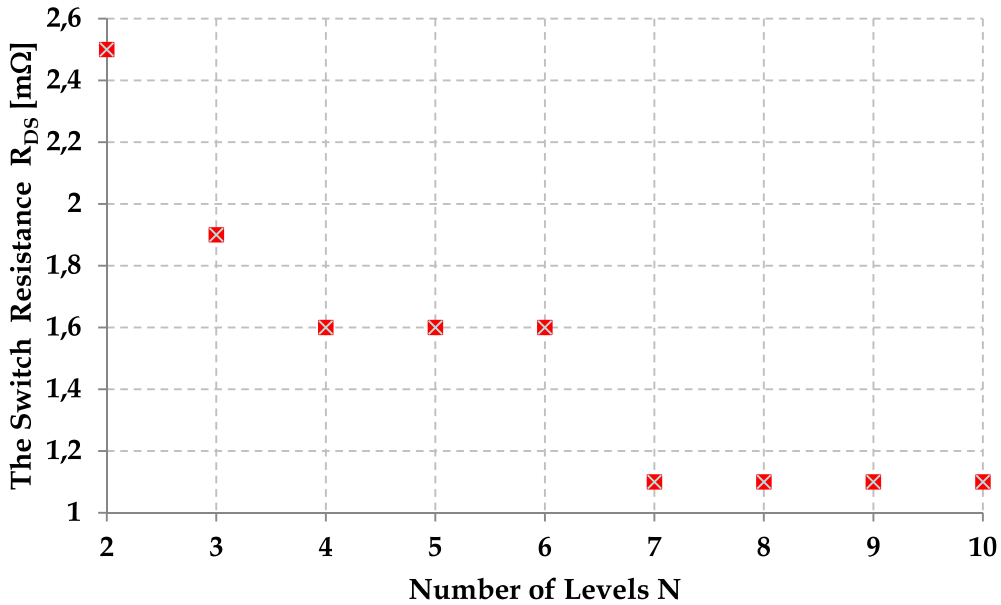
- **Infineon OptiMOS family**

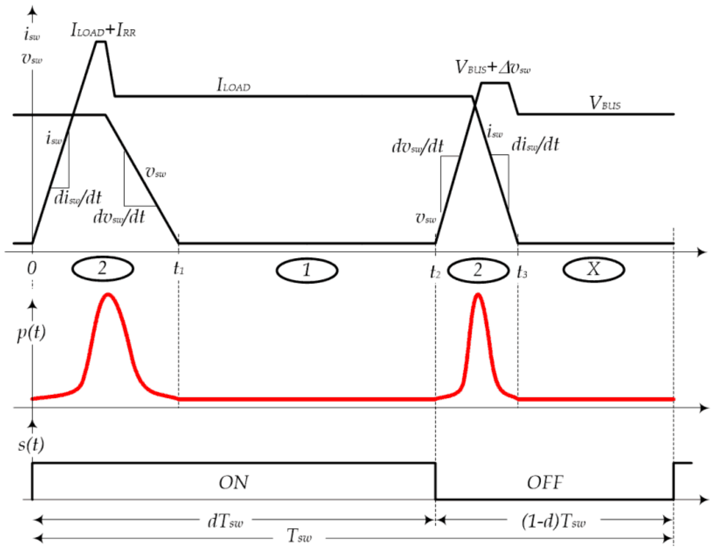
...Multi-level Converters...

1. Conduction Losses

$$P_{CON} = (N-1) I_0^2 R_{DS(N)}$$

- ❑ **Depend on number of Levels *N***
  - ❑ **R_{DS}= *Function* (The blocking voltage)**
  - ❑ **The blocking voltage=*Function* (*N*)**





Low voltage MOSFET resistance R_{DS} versus number of levels N.

- **Infineon OptiMOS family,**
- **V_{BUS}=48V**

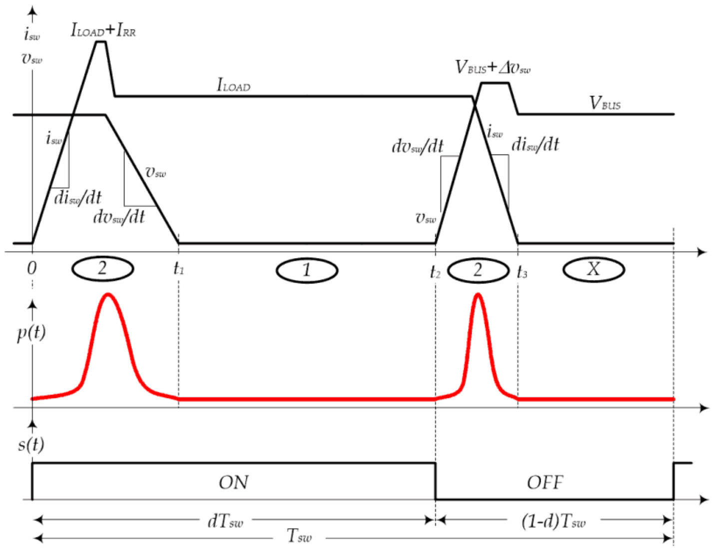
...Multi-level Converters...

1. Conduction Losses

$$P_{CON} = (N-1) I_0^2 R_{DS(N)}$$

2. The Switch Commutation Losses

i. Voltage/Current overleaping
ii. Parasitic Inductance
iii. Parasitic Capacitance



$$P_{SW} \cong \left\{ \underbrace{\frac{V_{BUS}}{(N-1)} I_0 \frac{(t_{iF}+t_{vR}+t_{iR}+t_{vF})}{2}}_{i} + \underbrace{\frac{1}{2} L_{\zeta} I_0^2}_{ii} + \underbrace{\frac{1}{2}\left[\frac{V_{BUS}}{(N-1)}\right]^2 C_{OSS}}_{iii} \right\} f_{SW}$$

3. The FWD Commutation Losses

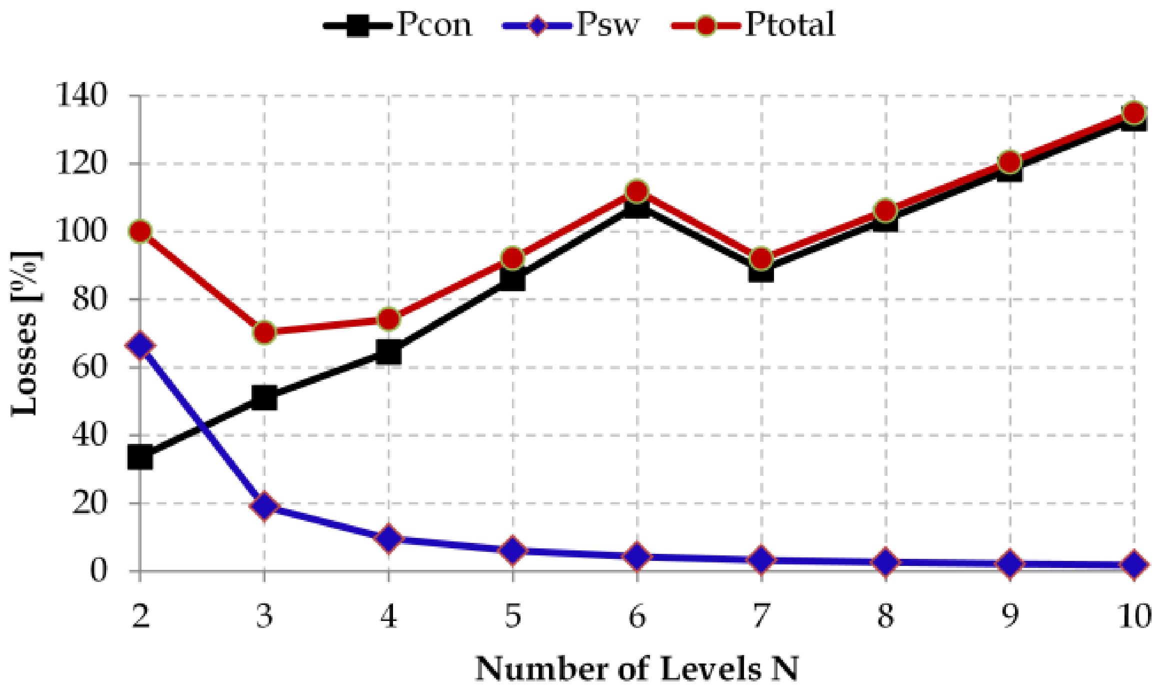
$$P_D \cong \left\{ \frac{V_{BUS}}{(N-1)} I_0 \frac{E_Q}{U_N I_N} \right\} f_{SW}$$

...Multi-level Converters...

Machine (HS-PMSG)

- **L_0=Constant**
- **f_{SW} can be scaled (reduced) to constant current ripple Δi_0**

$$f_{SW} = \frac{V_{BUS}}{L_0 (N-1) 4 \Delta i_{0\max}}$$



MOSFET losses versus number of levels *N*.

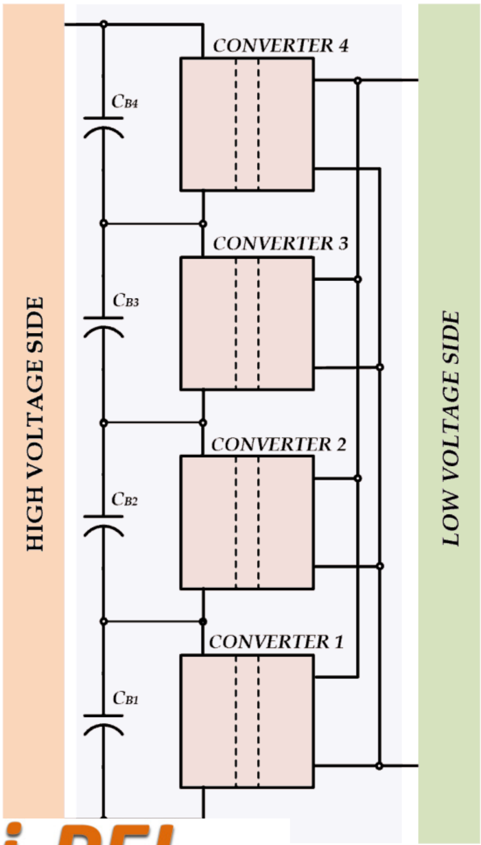
- **V_{BUS}=48V,**
- **I_0=150A,**
- **The switching frequency is scaled to constant current ripple Δi_0=20A.**

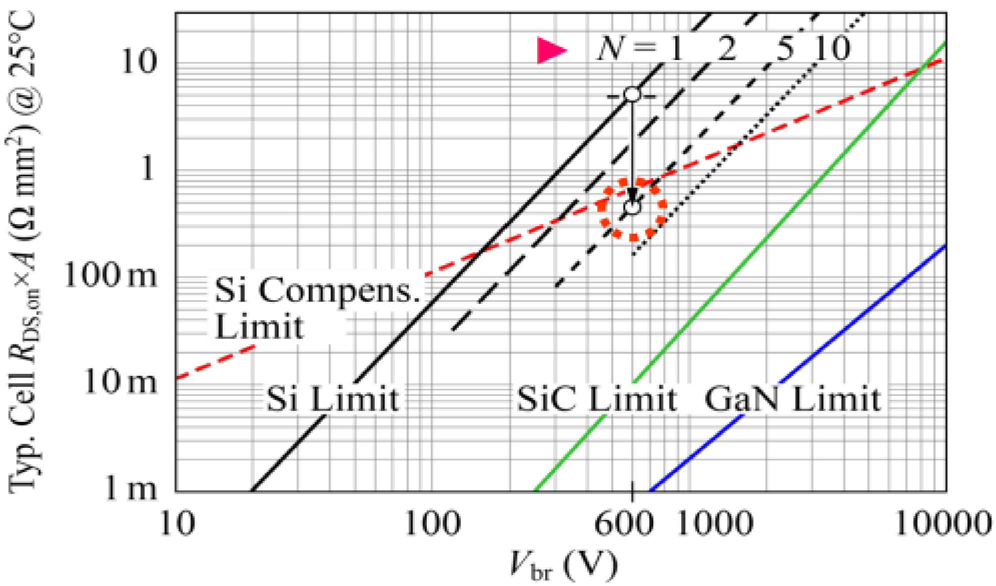
Multi-Cell & Multi-Level

-ISOP, IPOS,….-

...Multi-Cell & Multi-Level Converters…

- **High Voltage Side-Series connected converters**
- **Low Voltage Side-Parallel connected converters**

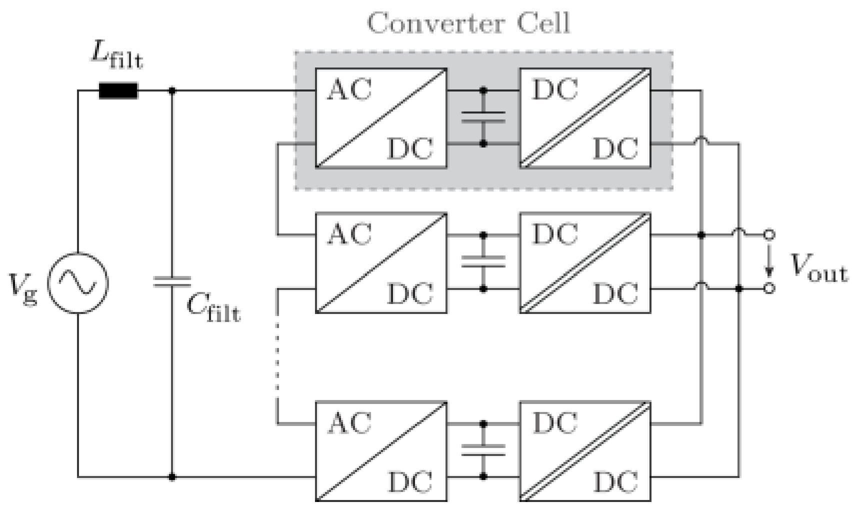


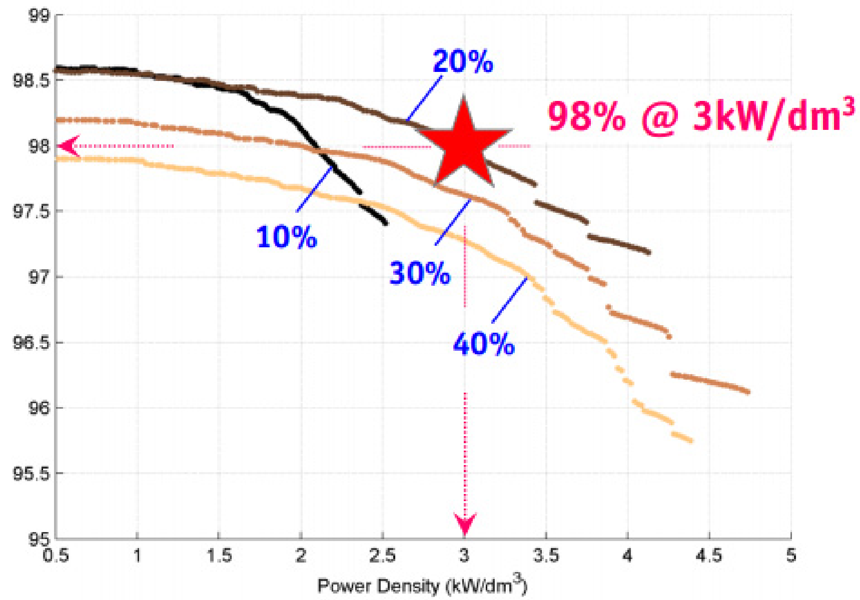


This is only way to go beyond limit of Si devices…

...Multi-Cell & Multi-Level Converters…

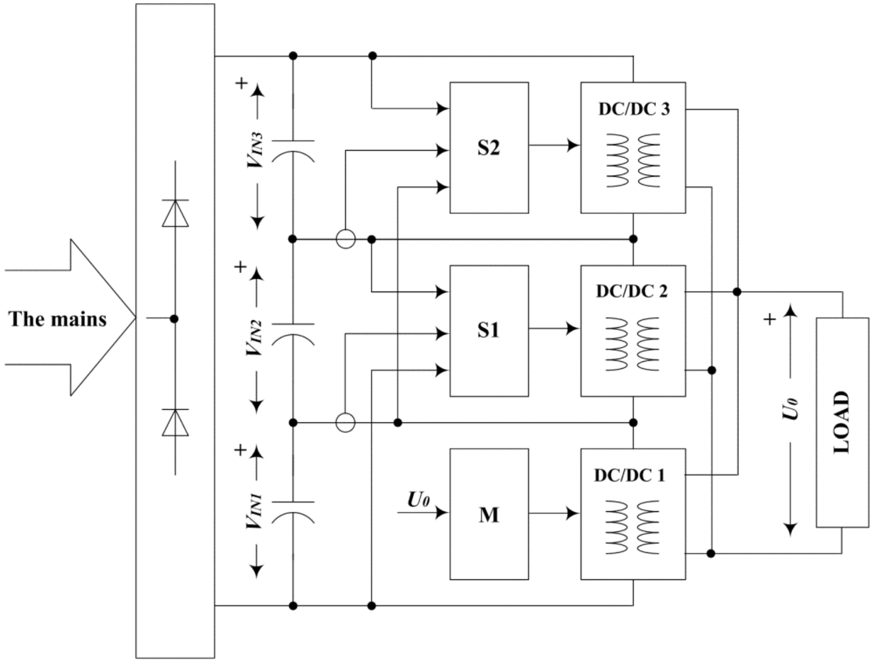
- ISOP based Ultra efficient and compact Telecom power supply



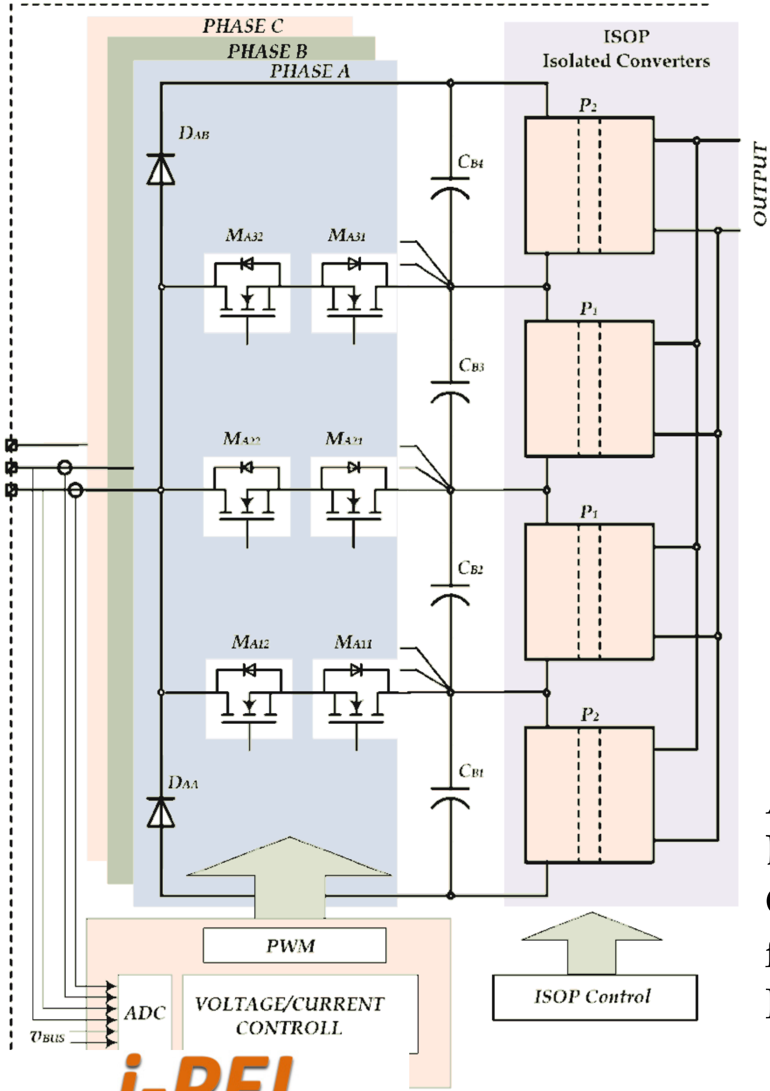


M. Kasper, J. W. Kolar and G. Deboy, "98.5% / 1.5kW/dm³ Multi-Cell Telecom Rectifier Module (230VAC/48VDC) –Breaking the Pareto Limit of Conventional Converter Approaches" ECPE Workshop "Advanced Multi-cell / Multi-level Power Converters", 1-2 July, 2014, Toulouse, France

Low Cost Auxiliary power supply based on ISOP Concept



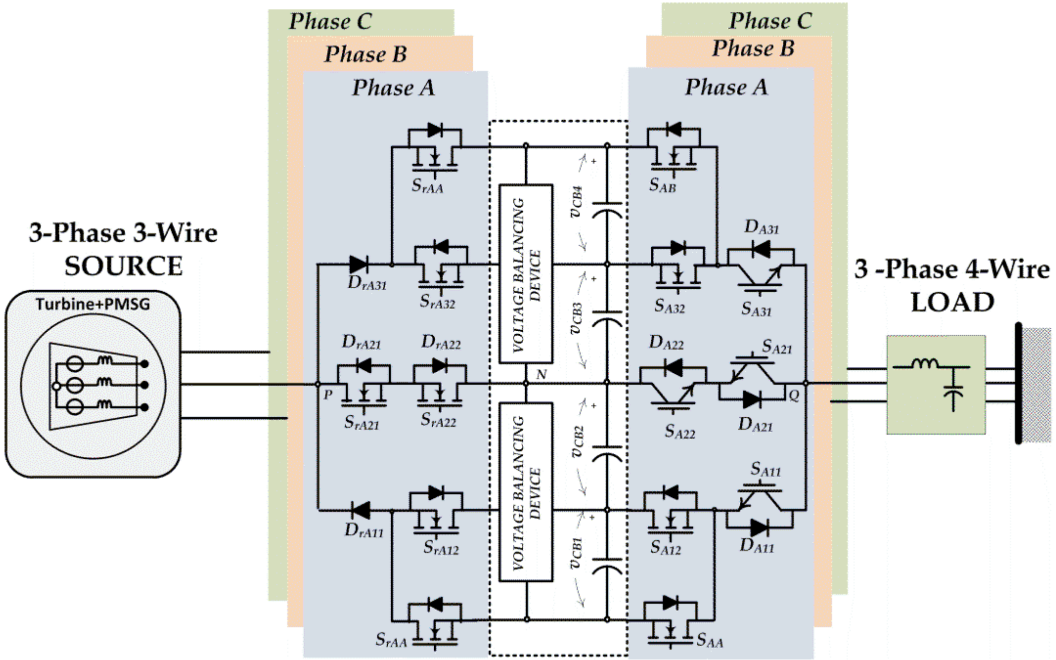
P. J. Grbović, "Input Serial Output Parallel (ISOP) Connected High Voltage Power Supplies Based on Simple Master/Slave Control Technique", *IEEE Trans. Power Electronics*, Vol. 24, No. 2, pp. 316-328, February 2009

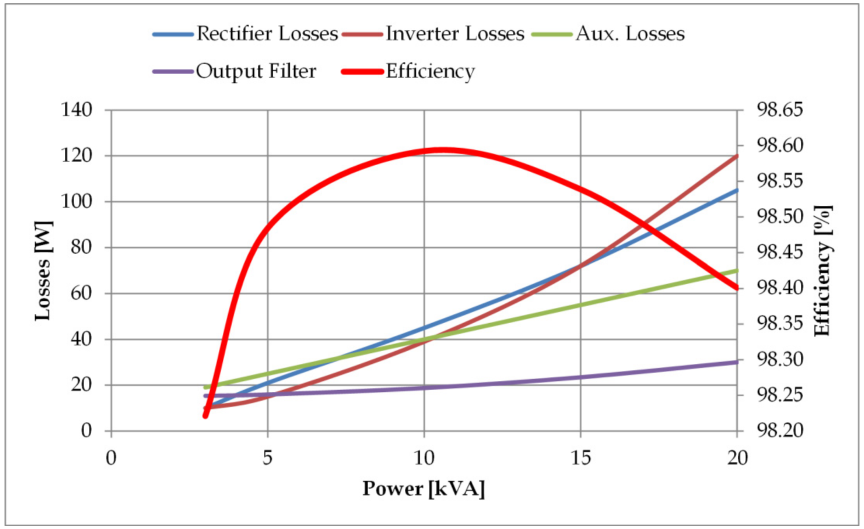


ISOP DC-DC Converter for Aerospace Applications

Alessandro Lidozzi, **Petar J. Grbović**, Luca Solero, Marco Di Benedetto and Stefano Bifaretti, "ISOP DC-DC Converters Equipped 5-Level Unidirectional T-Rectifier for Aerospace Applications" ECCE America 2015, Montreal, Canada, 20-24 September, 2015.

...Multi-Cell & Multi-Level Converters…





- P. J. Grbović , M. Di Benedetto, L. Solero, F. Crescimbini and A. Lidozzi, " **5-Level E-Type Back to Back Power Converters:** ***A New Solution for Extreme Efficiency and Power Density*** "
  - **98.5% Double Conversion Efficiency**
  - **5.3kW/dm^3**
  - **5kVA/kg**
  - **Si Devices Only (no WBG)**

At the End, Multi-Level…Multi-Cell…ISOP… Is it easy and good as it looks like??

universität innsbruck

...Some Issues…

Multi-Cell & Multi-level Conversion will solve all our issues….**or may be not**….

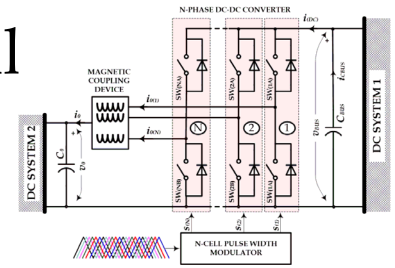
- 120V OptiMOS for 3 phase 400V system
  - **Very low losses**
  - **Very popular and low cost device**

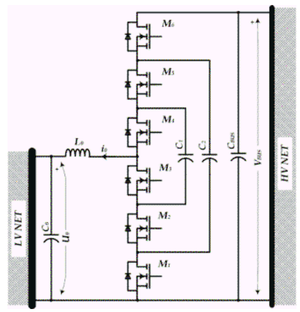
How many devices we need per a system?

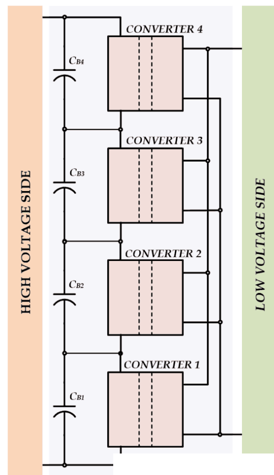
I. **2x10=20 per phase and cell**

II. **2 cells & 3 phases** → **120 devices per a converter**

III. **Back to back Config.** → **240 Devices per a system**



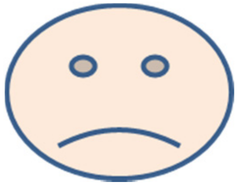


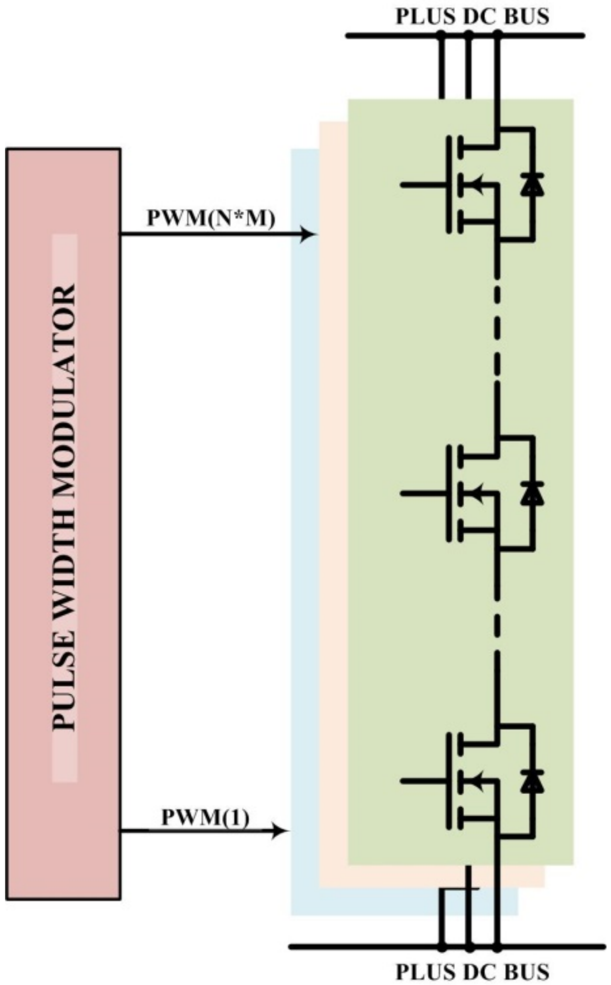


...Some Issues…

I. PULSE WIDTH MODULATOR

- Device=1 PWM
- 1 Converter =120 PWMs
- Traditionally *DSC TMS 335/337*
  - Max 24 PWMs
- DSC is not an Option

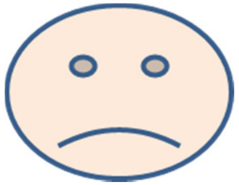




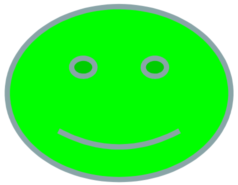
...Some Issues…

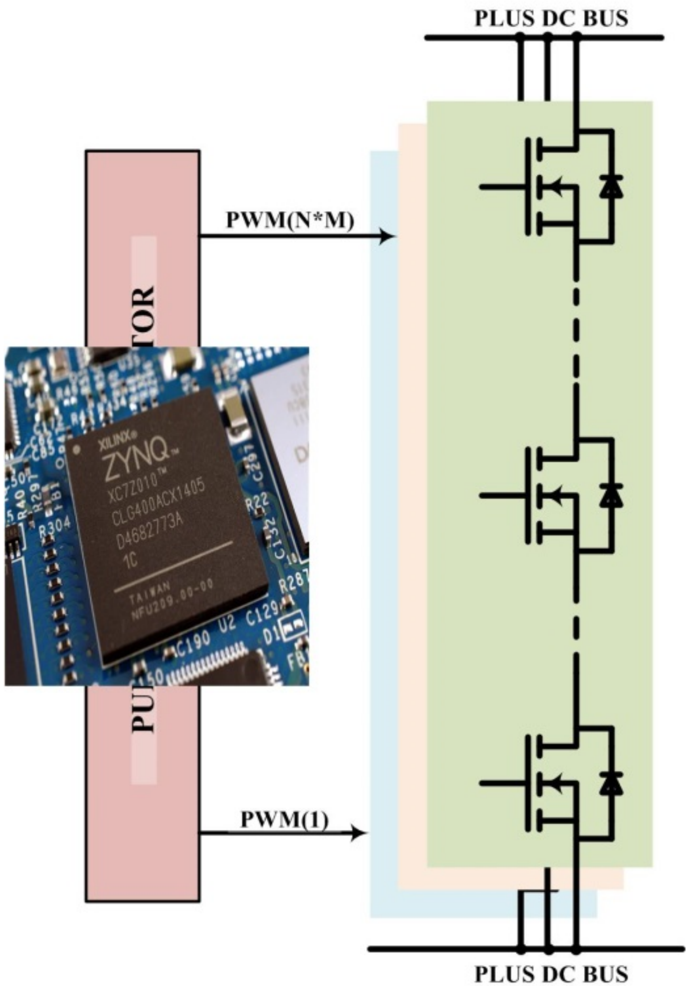
I. PULSE WIDTH MODULATOR

- Device=1 PWM
- 1 Converter =120 PWMs
- Traditionally *DSC TMS 335/337*
  - Max 24 PWMs
- DSC is not an Option



- Only Option is an FPGA or a CPLD

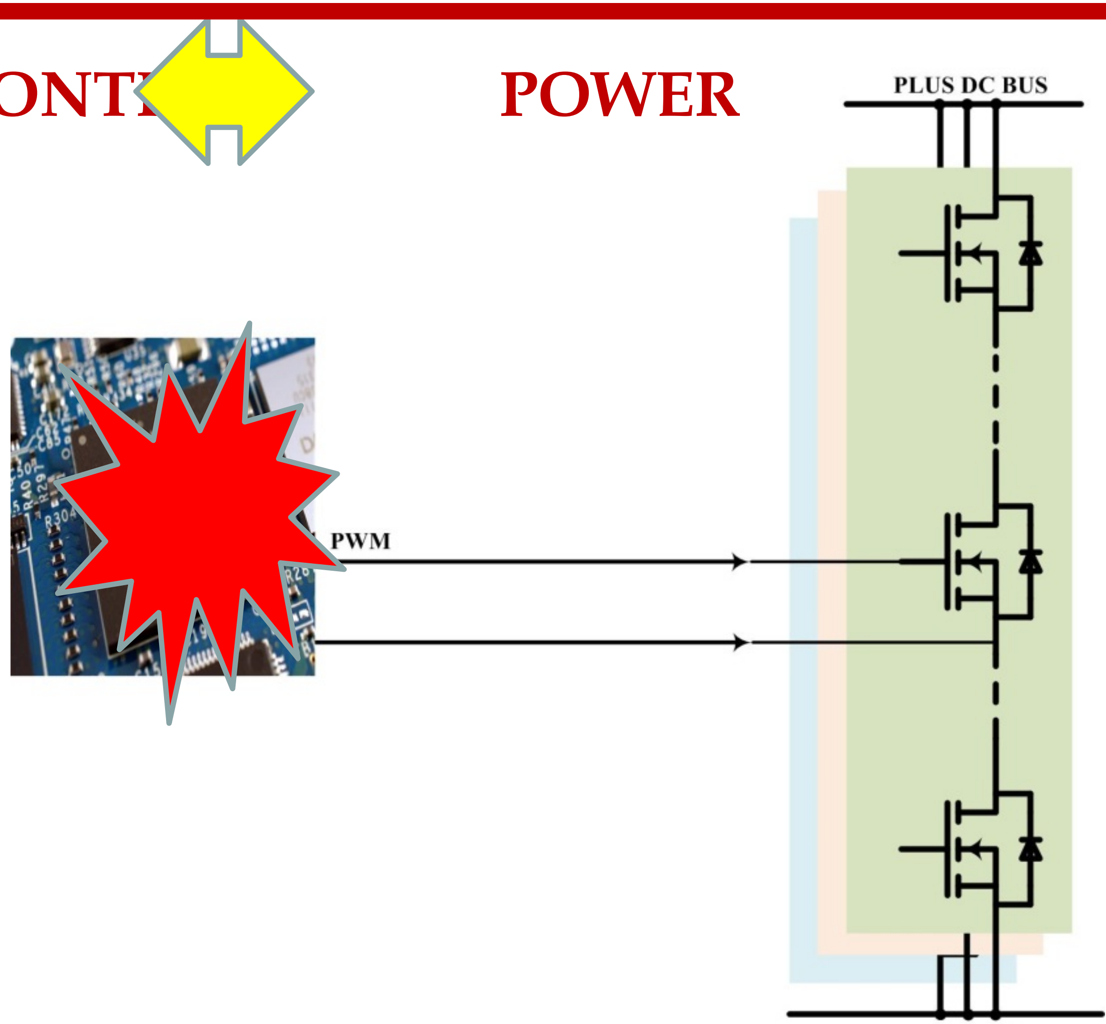




...Some Issues...

II. INTERFACE: CONT[illegible] POWER

- FPGA does not like direct connection to power device



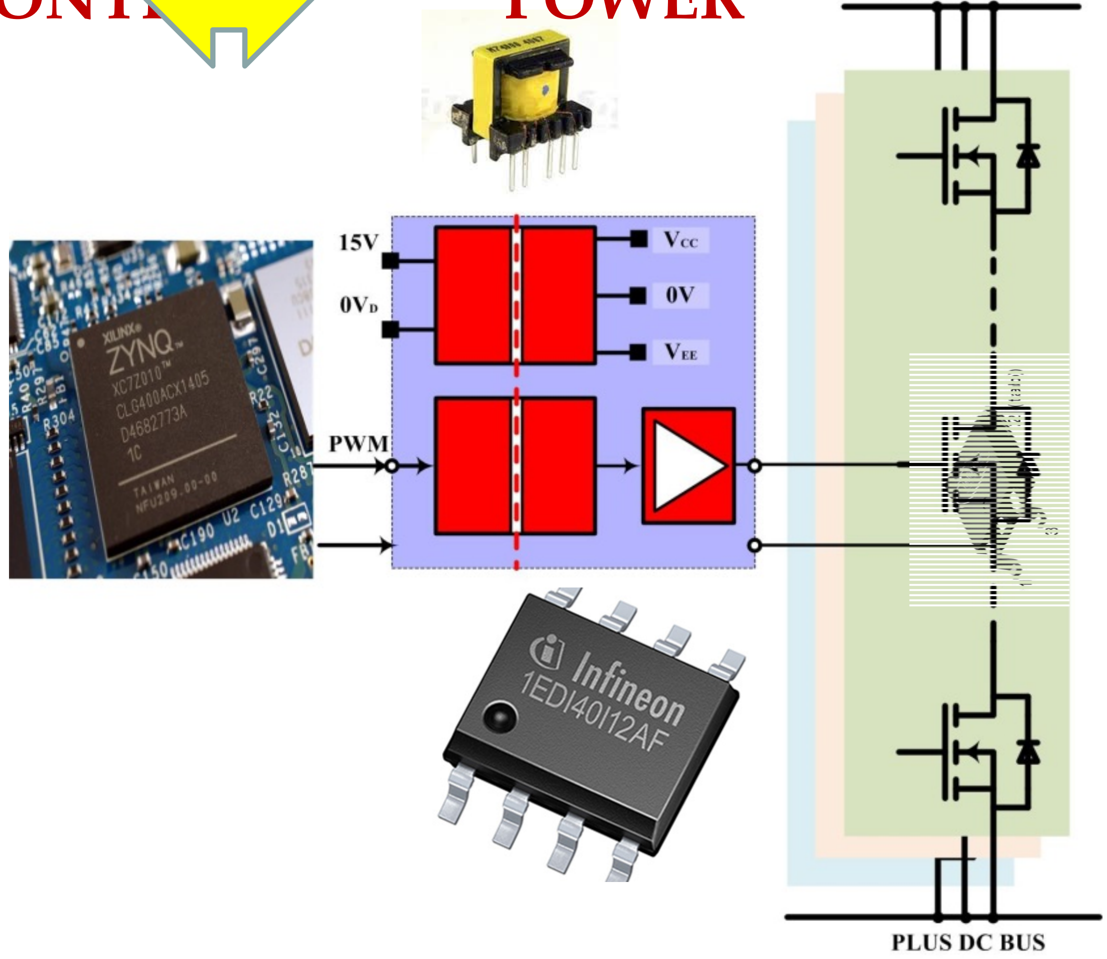
II. INTERFACE: CONT… POWER

- A Link between is a MUST

a) Iso.. Gate Driver,

b) Iso.. Power Supply

Today it is state of the art??



...Some Issues…

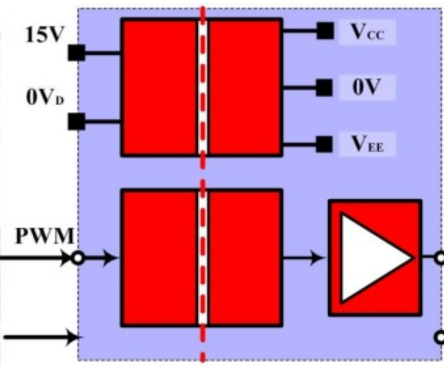
II. INTERFACE: CONTROL ⟺ POWER

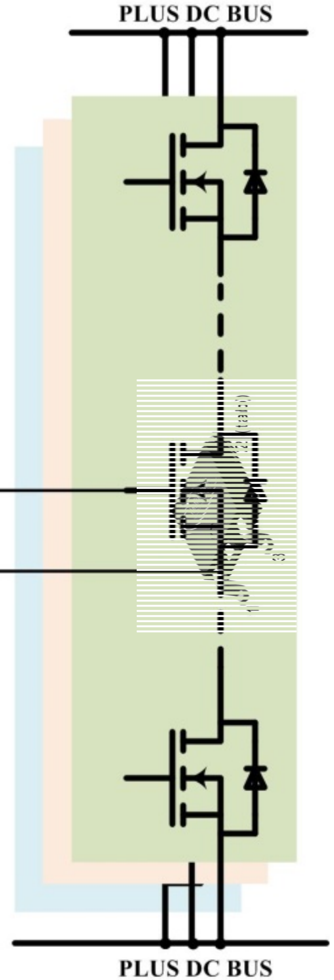
- A Link between is a MUST

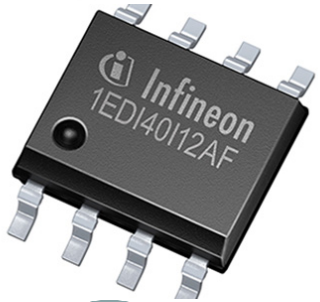
a) Iso.. Gate Driver,

b) Iso.. Power Supply

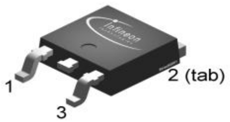
Today it is state of the art??







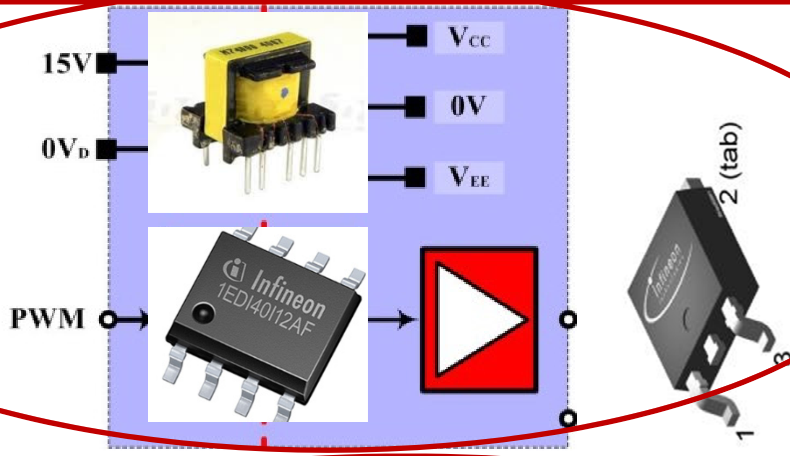
1 Device → 1 GD+PS → $$$$



>20% of total BOM cost

...Some Issues...

Today



???

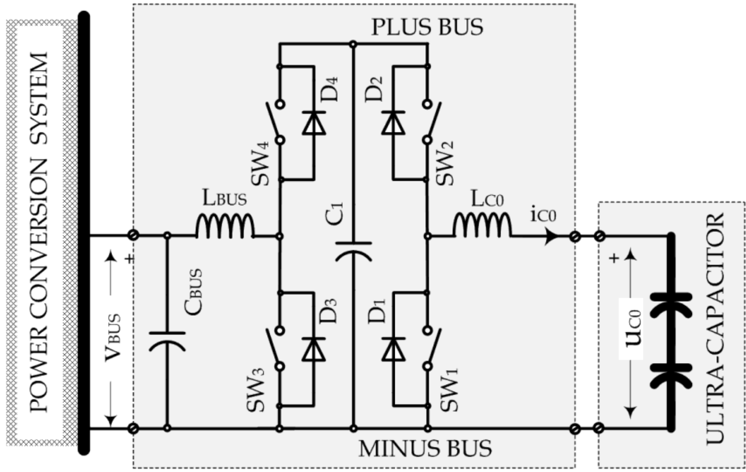
Tomorrow

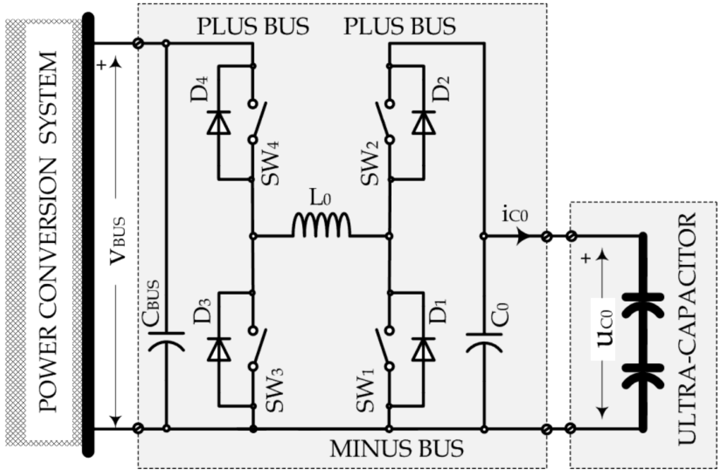
Buck-Boost Converters

Cascaded two level single-cell modules

- The voltage gain (***0<m<∞***)
- Double conversion, cost & losses

5. Boost-buck convertor
   - The input and output currents are continuous
   - Two inductors, one capacitor
     - Size and cost
   - The devices voltage rating
6. Buck-boost convertor
   - The input and output currents are discontinuous
   - Two capacitors, one inductor
     - Size and cost



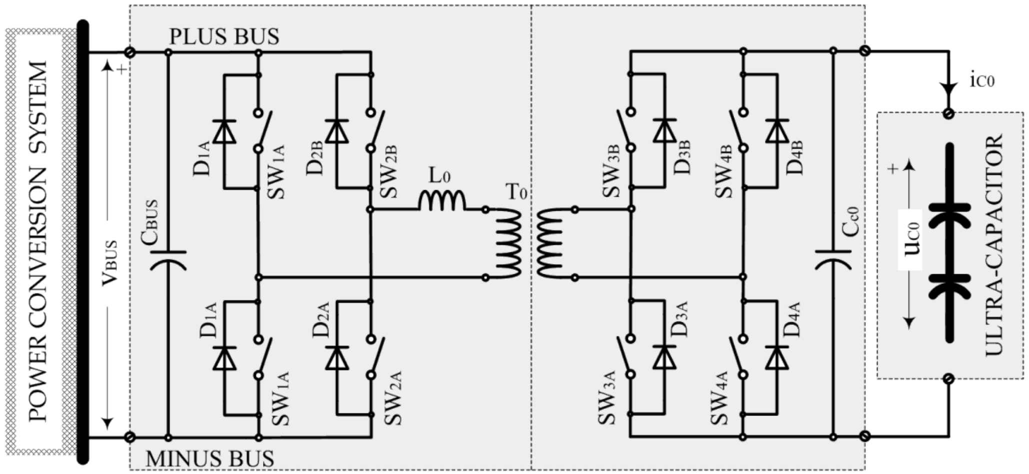


Isolated Converters

Isolated Converters

- Isolation
- High voltage ratio
- Complex and expensive

7. Single-Phase Double Active Bridge (DAB)

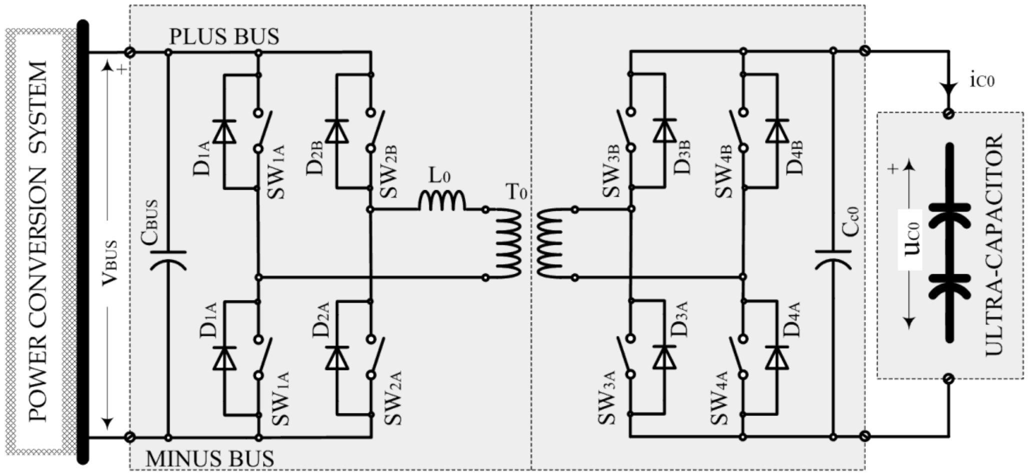


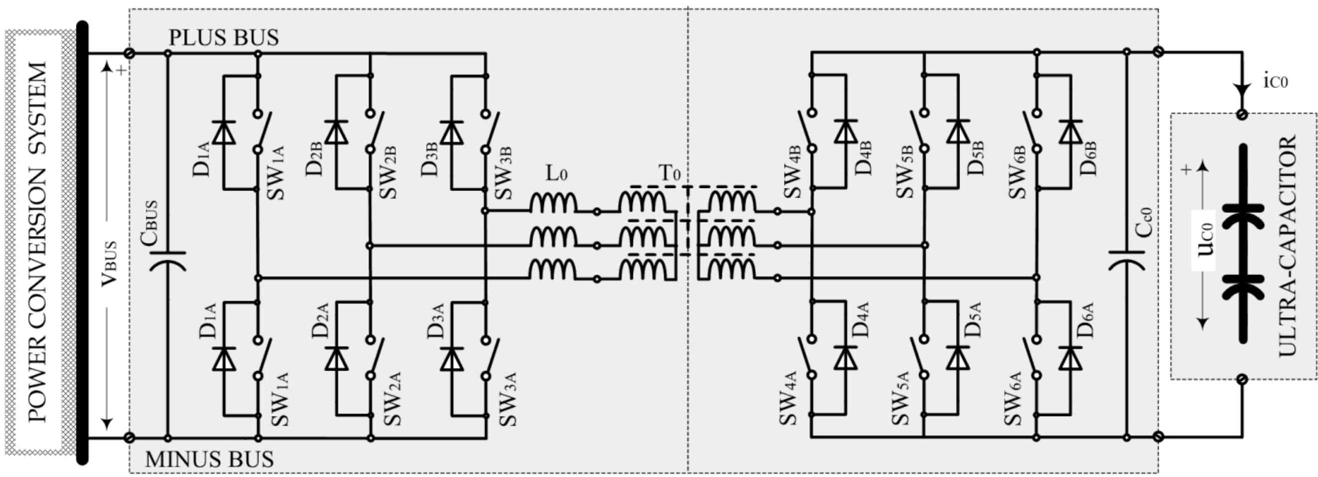
Isolated Converters

Isolated Converters

- Isolation
- High voltage ratio
- Complex and expensive

7. Single-Phase Double Active Bridge (DAB)
8. Three-Phase Double Active Bridge (DAB)





Application Summary & Discussion

Non-Isolated Interface Converters when galvanic isolation not required,

❑Two-Level Single-Cell & Multi-Cell Interleaved Converters:

- Medium & High Power Applications
- Low voltage applications, the DC bus voltage V_{BUS}<1400V
  - Switching frequency f_{SW}<20kHz
  - 600V, 1200V & 1700V IGBTs and PiN Diodes are used
  - **CollMOS used only in ZVS discontinuous conduction mode (DCM).**

Application Summary & Discussion

Non-Isolated Interface Converters when galvanic isolation not required,

❑Three-Level & Multi-level Converters are used in following cases:

- Low Voltage Applications, the DC bus voltage V_{BUS}<1400V
  - Low & Medium Power
  - High frequency & High power density applications
  - Switching frequency f_{SW}<20kHz
  - 600V & 1200V IGBTs and PiN Diodes are used
  - **CollMOS used only in ZVS discontinuous conduction mode (DCM).**
- Medium Voltage Applications
  - The dc bus voltage V_{BUS}>1400V
  - Switching frequency f_{SW}<10kHz
  - 1200V & 1700V IGBTs and PiN Diodes are used.

Application Summary & Discussion

- DC Side Connected ESS
  A. Partial Power Rated Converters
  B. Multi-Cell Interleaved Converters
  C. Multi-Level Converters
  D. Combination of the above

- AC Connected ESS (Grid Applications)
  A. CSC & Combination with Multi-Cell Converters
  B. PPRC & Combination with Multi-Cell/Level Converters

- EES with Isolation
  A. PPRC & Combination with ISOP ISO Converter (DC/DC)
  B. Multi-Level Rectifier & Combination with ISOP ISO Converter (AC/DC)

The Converter Design

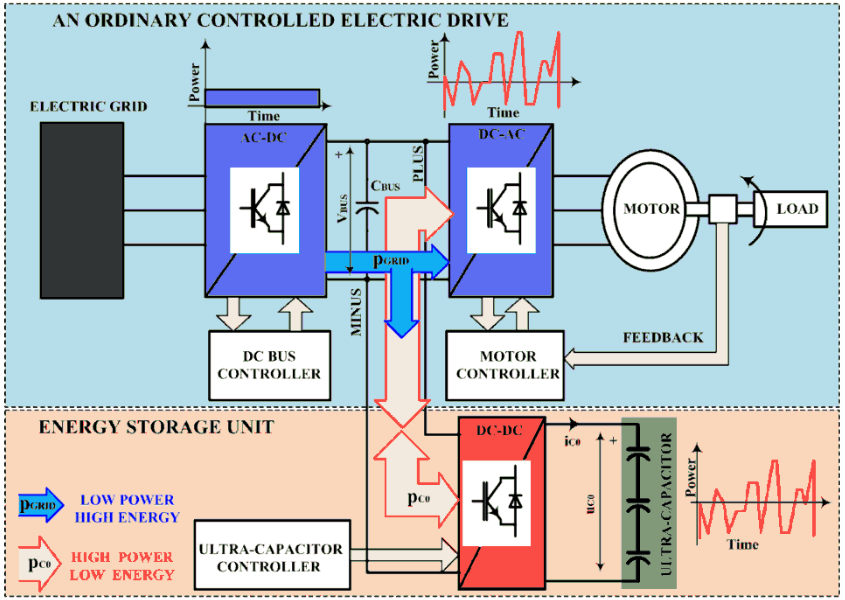
A Design Example 1:

-Three-Level Floating Output dc-dc Converter for Ultra capacitor Applications-

A Design Example 1:

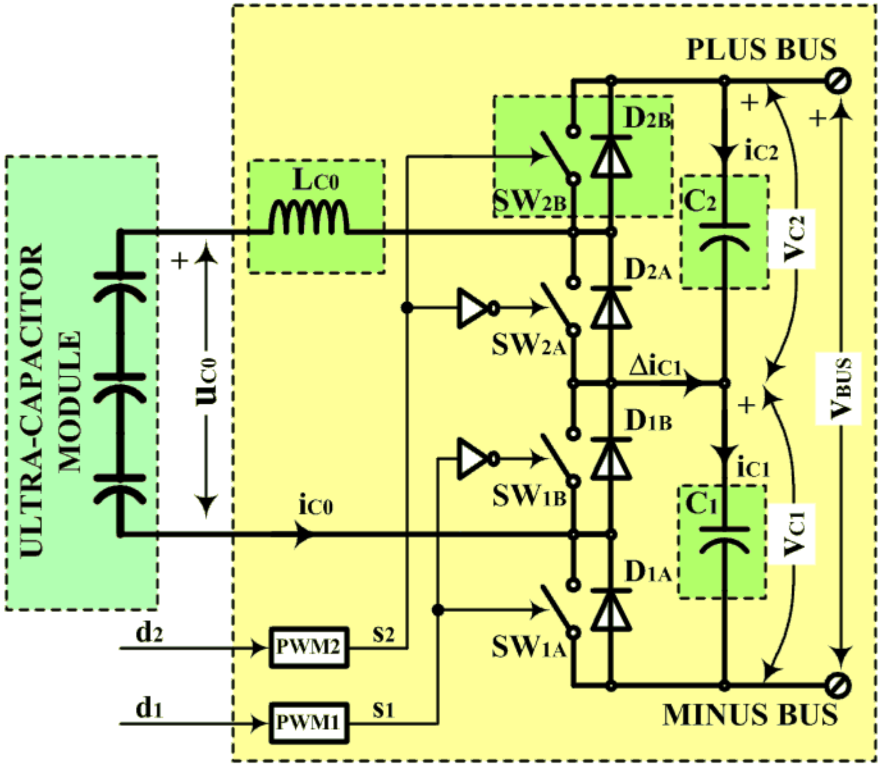
-Three-Level Floating Output dc-dc Converter

- The project "Application of ultra-capacitors in controlled electric drives" was sponsored by Schneider Toshiba Inverter, Pacy sur Eure, Franca and the Laboratoire d'Électrotechnique et d'Électronique de Puissance de Lille, l'Ecole Centrale de Lille, Villeneuve d'Ascq, France from 2007 until 2010.



The Converter Design

A design example: Three-level floating output dc-dc converter

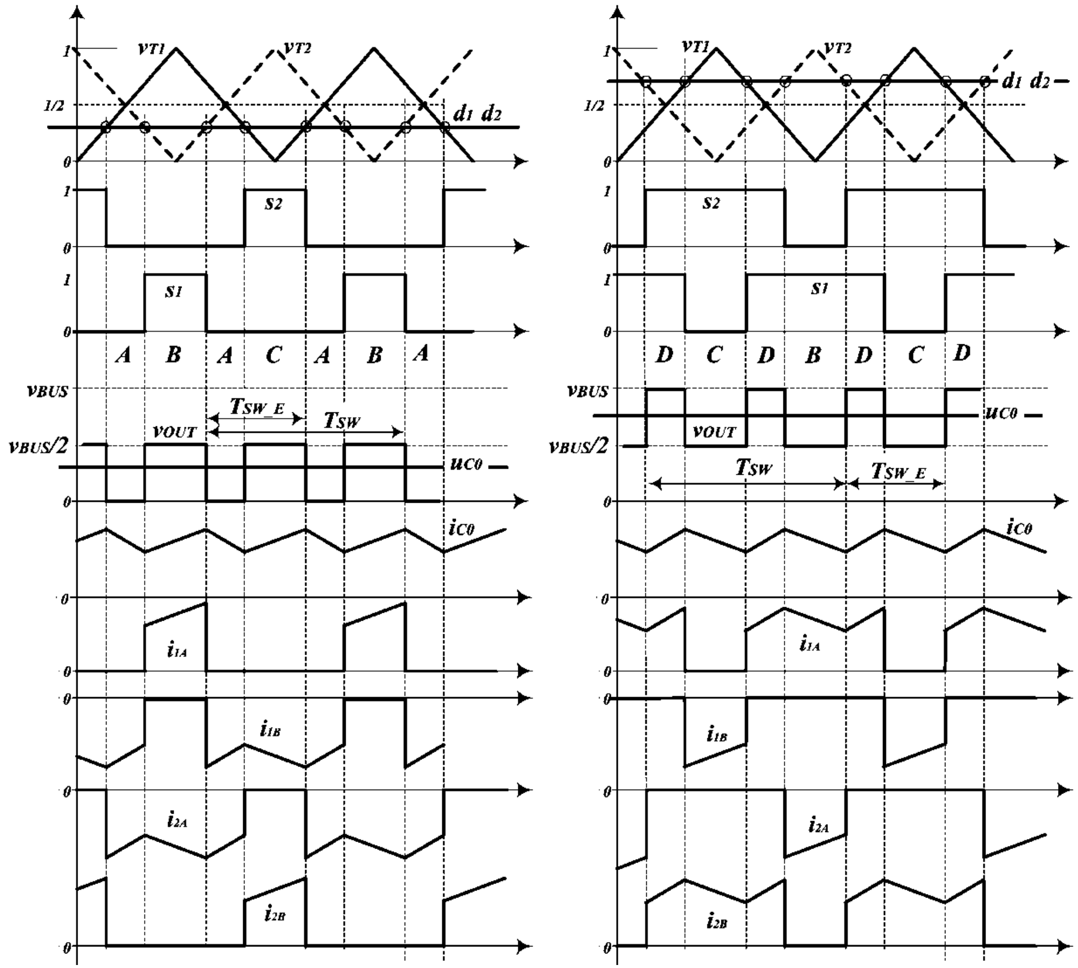


A. PWM strategy
   - Minimization of L_{C0} ***and*** C_1, C_2
   - Losses minimization
B. Selection and design of output filter inductor L_{C0}
C. Selection of input filter capacitors C_1 and C_2
D. Selection of semiconductor switches ***SW*** and freewheeling diodes ***D***
E. Cooling system design

The Converter Design

A. PWM strategy

- PWM carriers shifted for π radians
- Effective output frequency
- Reduced output current ripple and input voltage ripple
- The input voltages v_{C1} and v_{C2} balanced controlling duty cycles d_1 and d_2



The Converter Design

B. Selection and design of the output filter inductor L_{C0}

1. The inductance L_{C0}

$$L_{C0} \geq \frac{V_{BUS\max}}{\Delta i_{C0\max} f_{SW} 16}$$ at saturation current $$I_{C0sat} \cong \frac{P_{C0}}{U_{C0\min}} + \Delta i_{C0\max}$$

- Δi_{C0max} the current ripple, f_{SW} switching frequency

2. The inductor losses

$$P_{LC0}(P_{C0}, d) \cong \underbrace{R_{DC}\left(\frac{P_{C0}}{V_{BUS} d}\right)^2}_{Low\ frequency\ copper losses} + \underbrace{\left(R_{Cu(2f_{SW})} + R_{C(2f_{SW})}\right)\Delta i_{C0\max}^2 \frac{16}{3}\begin{cases}(1-2d)^2 d^2, & 0 \leq d \leq 1/2 \\ (2d-1)^2(1-d)^2, & 1/2 \leq d \leq 1\end{cases}}_{High\ frequency\ copper\ and\ core\ losses}$$

- Duty cycle when the ultra-capacitor is discharged with constant power P_{C0} from max operating voltage U_{C0max}

$$d \cong \frac{V_{BUS}}{U_{C0\max}}\sqrt{\frac{C_0 U_{C0\max}^2}{C_0 U_{C0\max}^2 + 2P_{C0} t}}$$

The Converter Design

C. Selection of the input filter capacitors C_1, C_2

1. The capacitance C

$$C \geq \max\left(\frac{P_{C0}}{V_{BUS}\Delta v_{BUS\max} f_{SW} 2}, \frac{P_{C0}\left(3-2\sqrt{2}\right)}{V_{BUS}\Delta v_{BUS\max} f_{SW} 2}\right)$$

- Δv_{BUSmax} the dc bus voltage ripple, f_{SW} switching frequency

2. The capacitor losses

$$P_C \cong \left(\frac{P_{C0}}{V_{BUS}}\right)^2 \frac{1-d}{d} R_{ESR} = \left(\frac{P_{C0}}{V_{BUS}}\right)^2 \frac{1-\frac{V_{BUS}}{U_{C0\max}}\sqrt{\frac{C_0 U_{C0\max}^2}{C_0 U_{C0\max}^2 + 2P_{C0}t}}}{\frac{V_{BUS}}{U_{C0\max}}\sqrt{\frac{C_0 U_{C0\max}^2}{C_0 U_{C0\max}^2 + 2P_{C0}t}}} R_{ESR}$$

- Duty cycle when the ultra-capacitor is discharged with constant power P_{C0} from max operating voltage U_{C0max}

The Converter Design

D. Selection of the semiconductor switches

1. Voltage rating

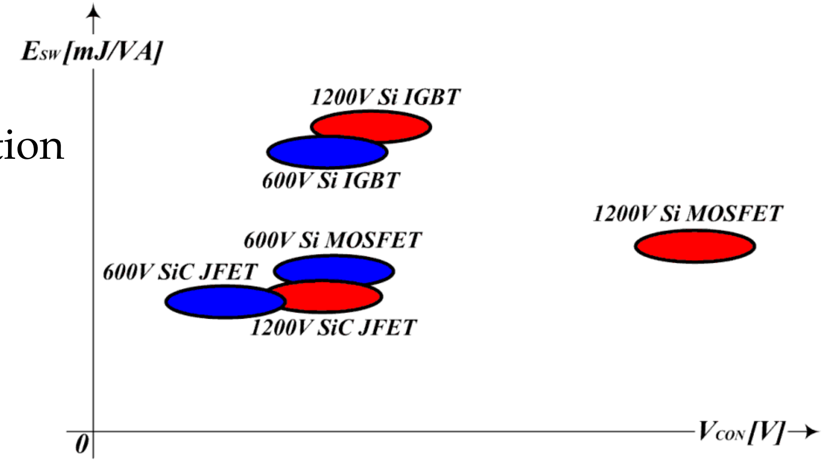
$$V_{SW\max} = V_{D\max} = \frac{V_{BUS\max}}{2} + \Delta V$$

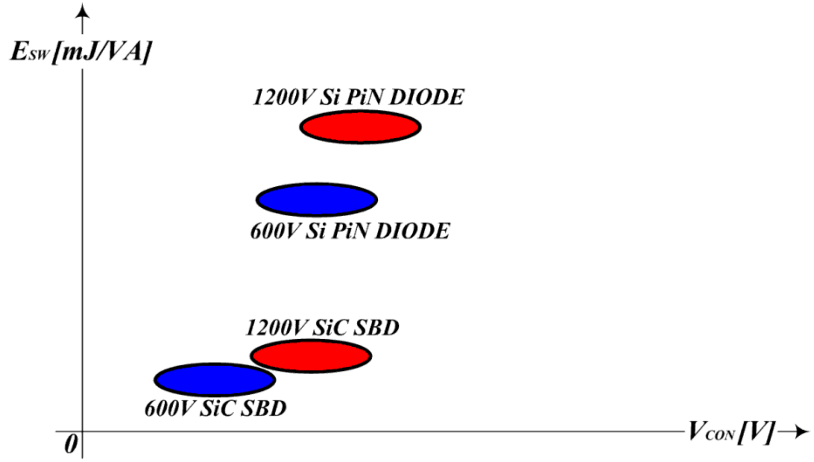
ΔV commutation over-voltage

2. Current rating

$$I_{SW\max} = I_{D\max} \geq \frac{P_{C0}}{U_{C0\min}} + \Delta i_{C0\max}$$

3. The device technology
   - Defined by the device voltage rating and switching frequency
     a) Si MOSFET, Si IGBT
     b) SiC JFET, SiC MOSFET
     c) Si PiN & SiC SBD



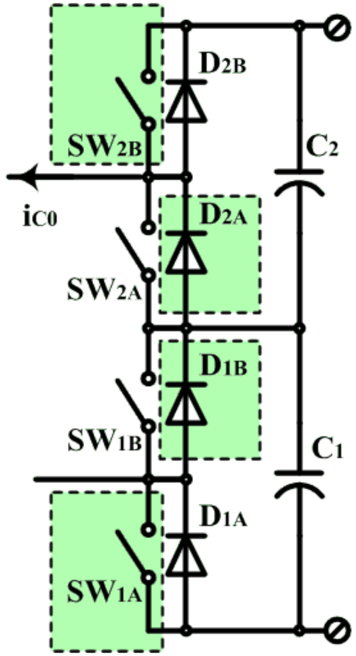


The Converter Design

D. Selection of the semiconductor switches

4. The device losses

- The current is positive, the switches SW_{1A} and SW_{2B}, and diodes D_{2A} and D_{1B} are conducting



$$P_{SW1A} = P_{SW2B} = \underbrace{\left(V_{SW0} \frac{P_{C0}}{V_{BUS}} + r_{SW} \frac{P_{C0}^2}{V_{BUS}^2 d} \right)}_{CONDUCTION} + \underbrace{\frac{1}{2} \frac{P_{C0}}{V_N I_N d} \left(E_{ON} + E_{OFF} \right) f_{SW}}_{SWITCHING}$$

$$P_{SW1B} = P_{SW2A} = 0$$

$$P_{D2A} = P_{D1B} = \underbrace{\left(V_{D0} \frac{P_{C0}}{V_{BUS}} + r_D \frac{P_{C0}^2}{V_{BUS}^2 d} \right) \frac{(1-d)}{d}}_{CONDUCTION} + \underbrace{\frac{1}{2} \frac{P_{C0}}{V_N I_N d} E_Q f_{SW}}_{SWITCHING}$$

$$P_{D1A} = P_{D2B} = 0$$

$V_{SW0},\ r_{SW},\ E_{ON},\ E_{OFF}$

$V_{D0},\ r_D,\ E_Q$

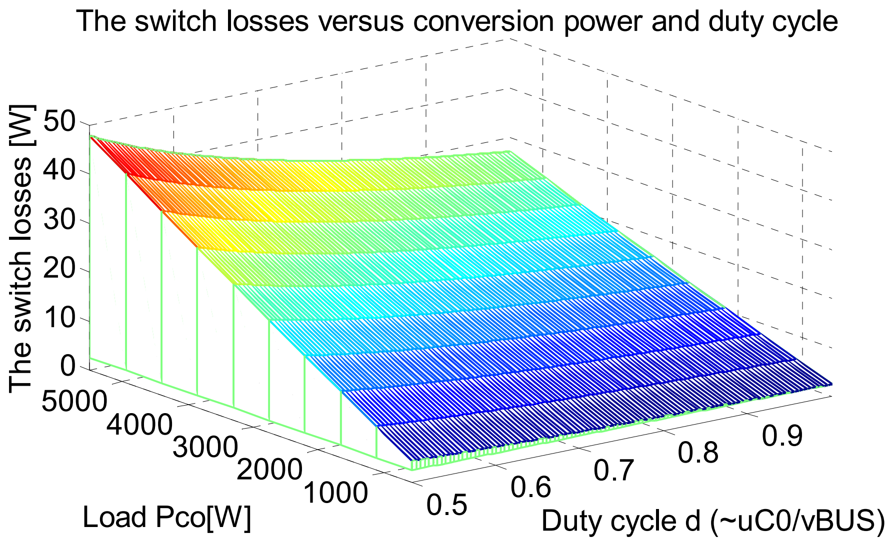
The device static and switching parameters

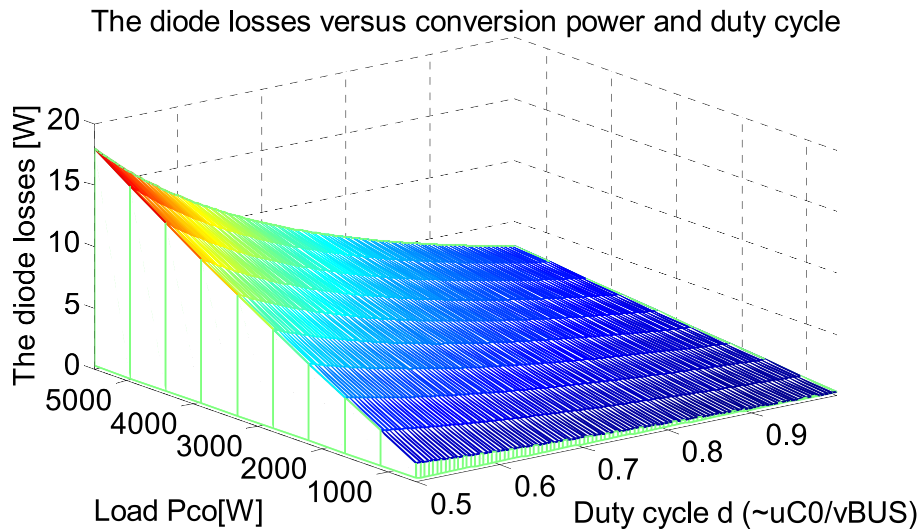
The Converter Design Example

Nominal power	P_{C0}=5500W
DC bus nominal voltage	V_{BUS}=700V
Ultra-capacitor max voltage	U_{C0max}=700V
Ultra-capacitor min voltage	U_{C0min}=350V
Switching frequency	f_{SW}=25kHz
The current ripple	Δi_{C0}=3A

IGBT/FWD 600V 30A						
V_{SW}	r_{SW}	*E_{ON}+E_{OFF}		V_{D0}	r_D	*E_Q
0.8V	27mΩ	80µJ/A		0.9 V	20 mΩ	10µJ/A
*Switching losses at V_N=300V T_J=150˚C						
FILTER INDUCTOR L_{C0}				CAPACITOR C_1, C_2		
High Flux Powder Core (2x) 58192-A2				MKP EPCOS B32774D4106		
L	R_{DC}	R_{AC}	R_C	C_1, C_2		ESR
580µH	38mΩ	0.8Ω	3Ω	2x10µF		3.75mΩ

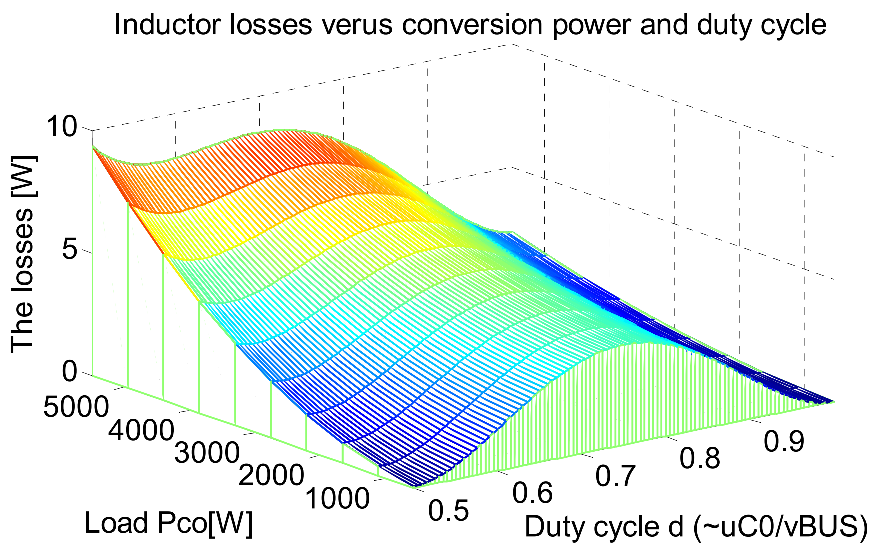
The Converter Design Example

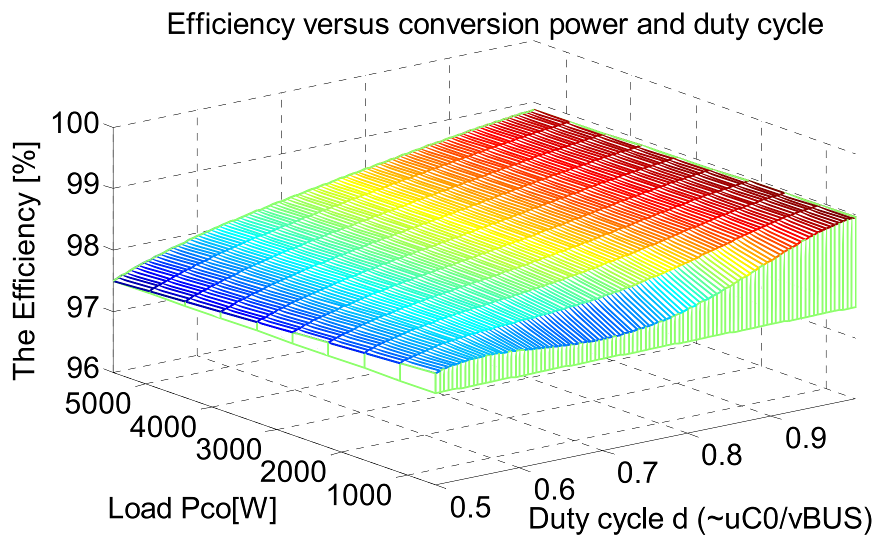




The switches SW_{1A}, SW_{2B} and diodes D_{1B} and D_{2A} losses. The dc bus voltage V_{BUS}=700V, switching frequency f_{SW}=25kHz

The Converter Design Example





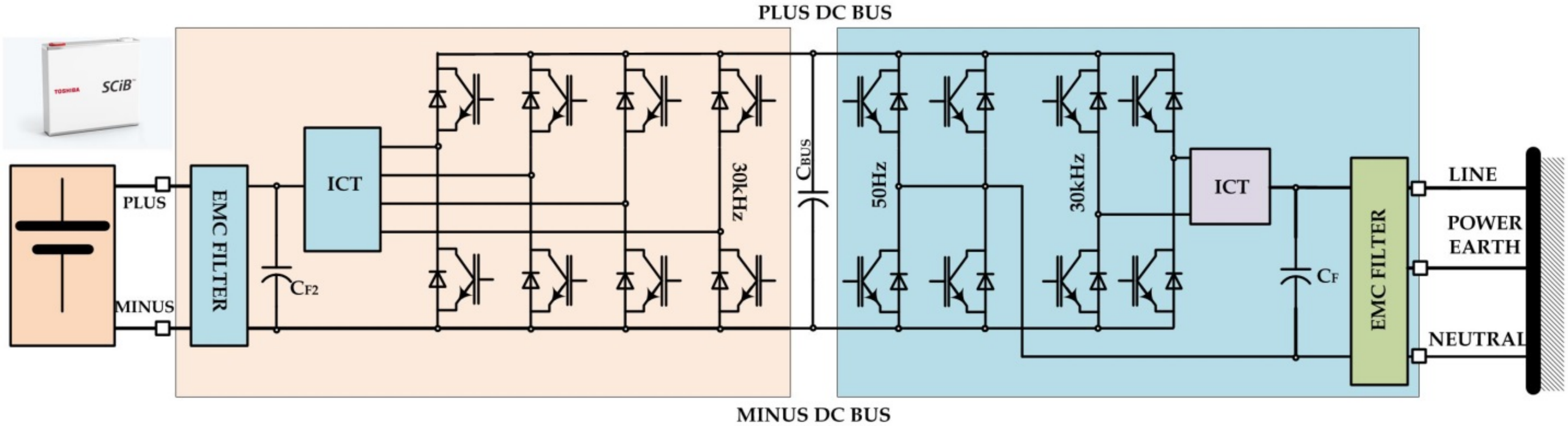
The inductor total losses and the converter efficiency . The dc bus voltage V_{BUS}=700V, switching frequency f_{SW}=25kHz

A Design Example 2:

-Four-Cell dc-dc Converter for Battery Grid Connected Single Phase Applications-

The Converter Design

Grid Side Converter		Battery Side Converter	
Grid Nominal Voltage	202 [V]	Battery Nominal Voltage	200 [V]
Nominal Power	10[kVA]	Battery Min. Voltage	144 [V]
Nominal Frequency	50 [Hz]	Rated Power	10 [kW]
THDi	<3%		
Power Factor	Any		



The Converter Design

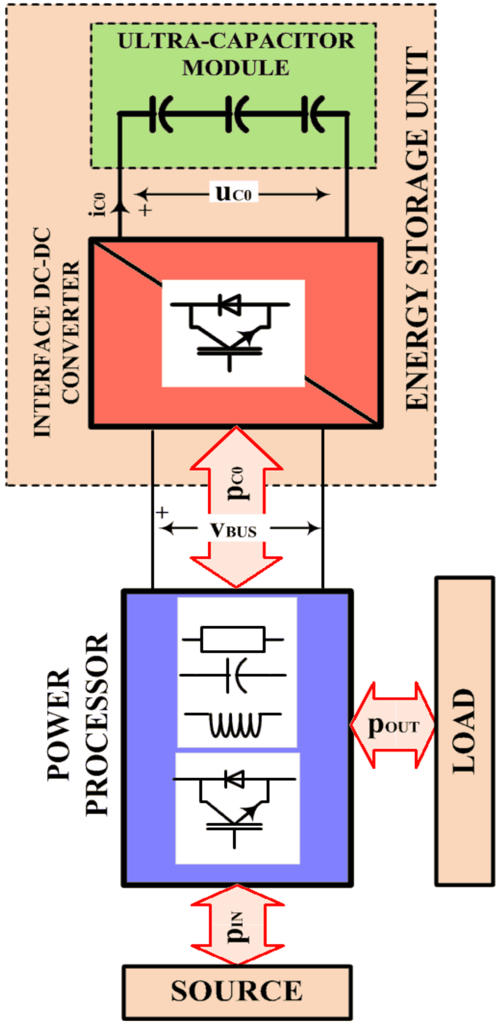
Grid Side Converter		Battery Side Converter	
Grid Nominal Voltage	202 [V]	Battery Nominal Voltage	200 [V]
Nominal Power	10[kVA]	Battery Min. Voltage	144 [V]
Nominal Frequency	50 [Hz]	Rated Power	10 [kW]
THDi	<3%		
Power Factor	Any		

Microsoft Excel Worksheet

The Converter Control

The Control Objective(s)

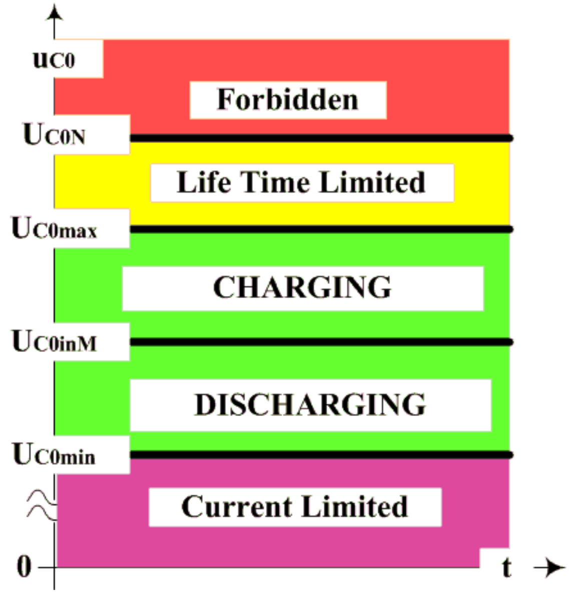
1. Low level converter control (state of the art ☺)
   - PWM and protection
   - Voltage balancing (Multi-Level converter)
   - Current balancing (Multi-Cell interleaved converter)
2. The ES current control (state of the art ☺)
   - Current limitation
3. The ES voltage control
   - State of charge (SOC) control
4. The conversion process control
   - The power processor input or output power (p_{IN}, p_{OUT}) control
   - Not necessarily coupled with the power processor control



The Converter Control

The ultra-capacitor voltage control

1. SOC~ the ultra-capacitor voltage u_{C0}
2. Whenever it is possible, regulate u_{C0} at intermediate level U_{C0inM}
   - U_{C0inM} determined by the application parameters (4.3)
   - Controlling u_{C0} at U_{C0inM} gives maximum flexibility of the power conversion system
3. Limit the ultra-capacitor voltage at maximum operating voltage U_{C0max}
4. Limit the ultra-capacitor voltage at minimum operating voltage U_{C0min}

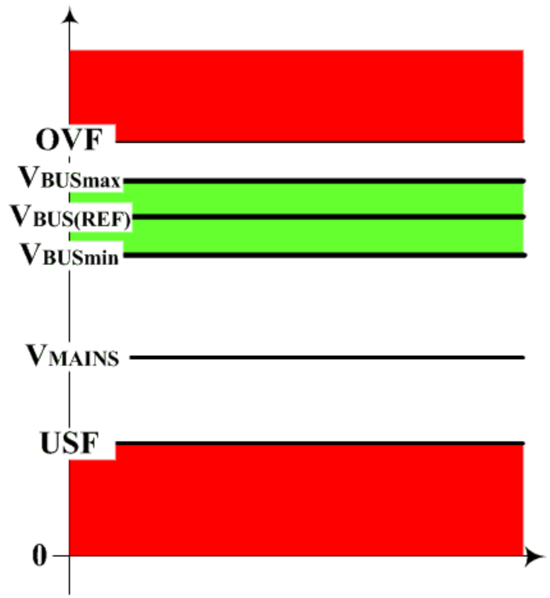


The Converter Control

The conversion process control

- Numerous possibilities for the power process control
- Control via the common dc bus voltage one of the simplest control schemes [4]

1. The power processor controls the dc bus voltage at the reference $V_{BUS(REF)}$
   - $V_{BUS(REF)}$ is fixed or flexible, defined by the power processor or the conversion process
2. Whenever it is necessary, the ultra-capacitor converter controls the dc bus voltage to lower reference $V_{BUS(min)}$ or upper reference $V_{BUS(max)}$.
   - $V_{BUS}=V_{BUS(max)}$ The ultra-capacitor is charged
   - $V_{BUS}=V_{BUS(min)}$ The ultra-capacitor is discharged
3. The bands $\Delta V_1=V_{BUS(REF)}-V_{BUS(min)}$ and $\Delta V_2=V_{BUS(max)}-V_{BUS(REF)}$ are small enough to be acceptable by the power processor



$V_{BUS(REF)}<V_{BUS(max)}$

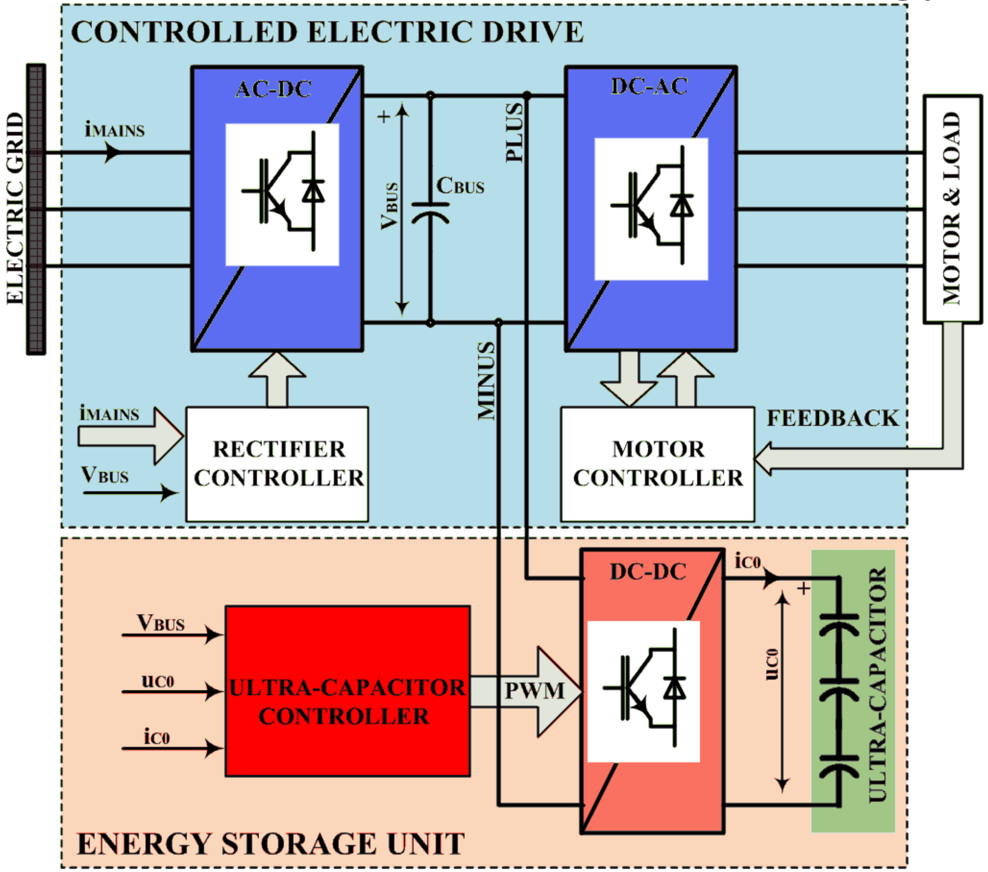
$V_{BUS(REF)}>V_{BUS(min)}$

USF Under supply fault

OVF Overvoltage fault

The Converter Control

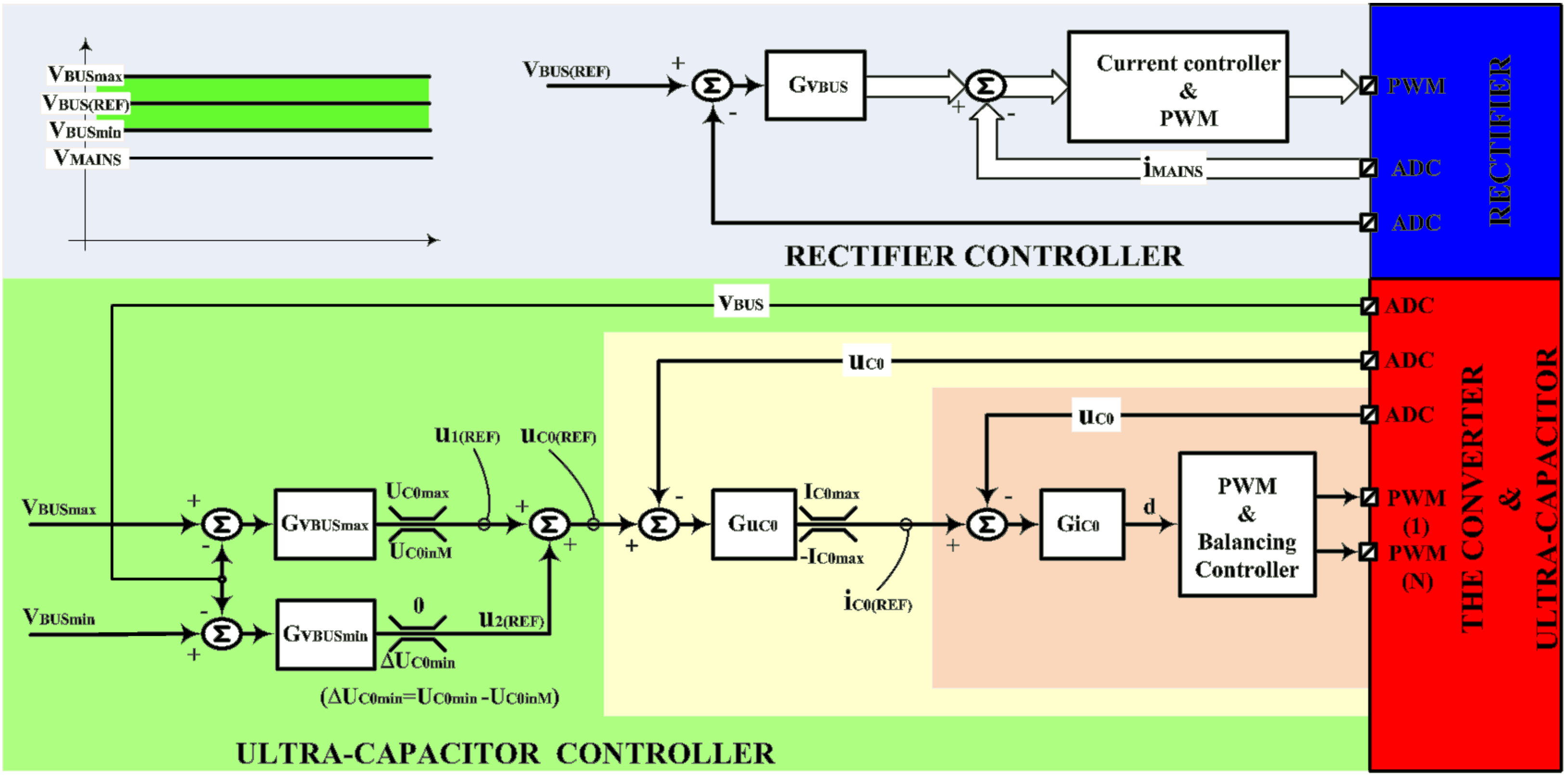
An example: Controlled electric drive with ultra-capacitor energy storage



- The rectifier (AC-DC) controls the dc bus voltage at the reference $V_{BUS(REF)}$
- The dc-dc converter controls the dc bus voltage at lower or upper reference and charges/discharges the ultra-capacitor
- The ultra-capacitor controller is independent of the rectifier controller
  - References must be set as

$$V_{BUS(min)} < V_{BUS(REF)} < V_{BUS(max)}$$

The Converter Control

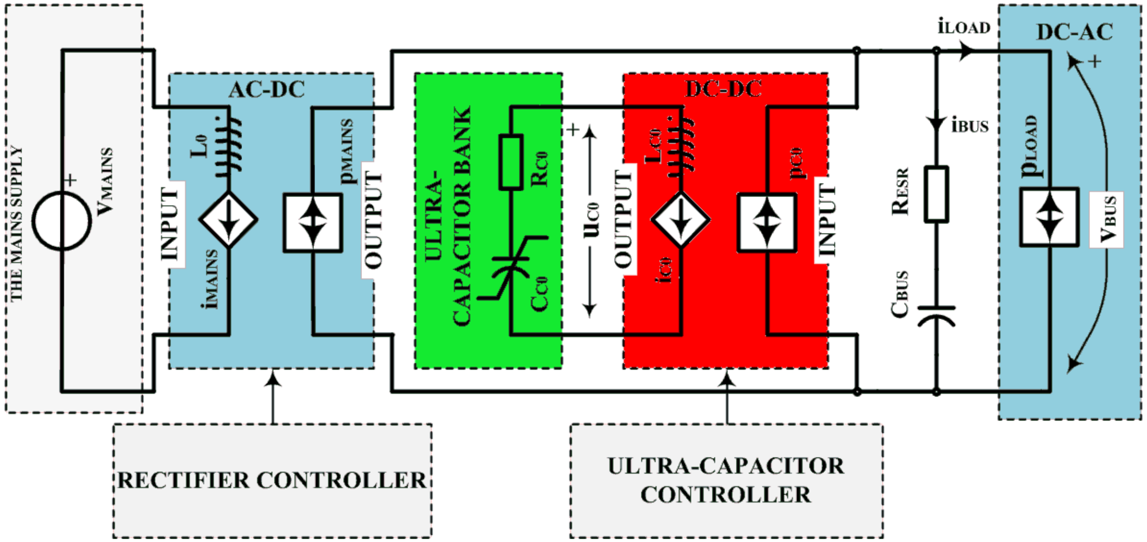


Control schema of an ultra-capacitor energy storage unit applied on a controlled electric drive [4]

The Converter Control

Large signal (non-linear) model

- Controlled power sources p_{MAINS}, p_{C0} p_{LOAD}
- Control variables i_{MAINS} and i_{C0}
- Disturbances v_{MAINS} and p_{LOAD}



$$C_{BUS}\frac{dv_B}{dt}=\frac{p_{MAINS}}{v_{BUS}}-\frac{p_{C0}}{v_{BUS}}-\frac{p_{LOAD}}{v_{BUS}}$$

$$p_{MAINS}=v_{MAINS}i_{MAINS}$$

$$p_{C0}=u_{C0}i_{C0}+\underbrace{i_{C0}L_{C0}\frac{di_{C0}}{dt}}_{\cong 0}$$

$$(C_0+2k_Cu_C)\frac{du_C}{dt}=i_{C0}$$

$$u_{C0}=u_C+R_{C0}i_{C0}$$

$$v_{BUS}=v_B+R_{ESR}\left(\frac{p_{REC}}{v_{BUS}}-\frac{p_{C0}}{v_{BUS}}-\frac{p_{LOAD}}{v_{BUS}}\right)$$

The Converter Control

Small signal (linear) model

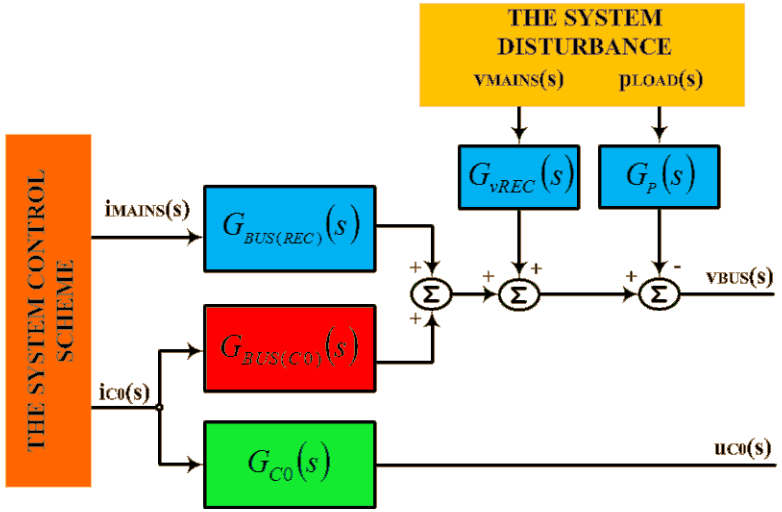
- Linearization & small signal model
- The controllers synthesis

$$\begin{bmatrix} u_{C0}(s) \\ v_{BUS}(s)\end{bmatrix} = \begin{bmatrix} G_{C0}(s) & 0 \\ G_{BUS(C0)}(s) & G_{BUS(MAINS)}(s)\end{bmatrix}\underbrace{\begin{bmatrix} i_{C0}(s)\\ i_{MAINS}(s)\end{bmatrix}}_{CONTROL} + \begin{bmatrix}0 & 0\\ G_P(s) & G_{vMAINS}(s)\end{bmatrix}\underbrace{\begin{bmatrix}p_{LOAD}(s)\\ v_{MAINS}(s)\end{bmatrix}}_{DISTURBANCE}$$

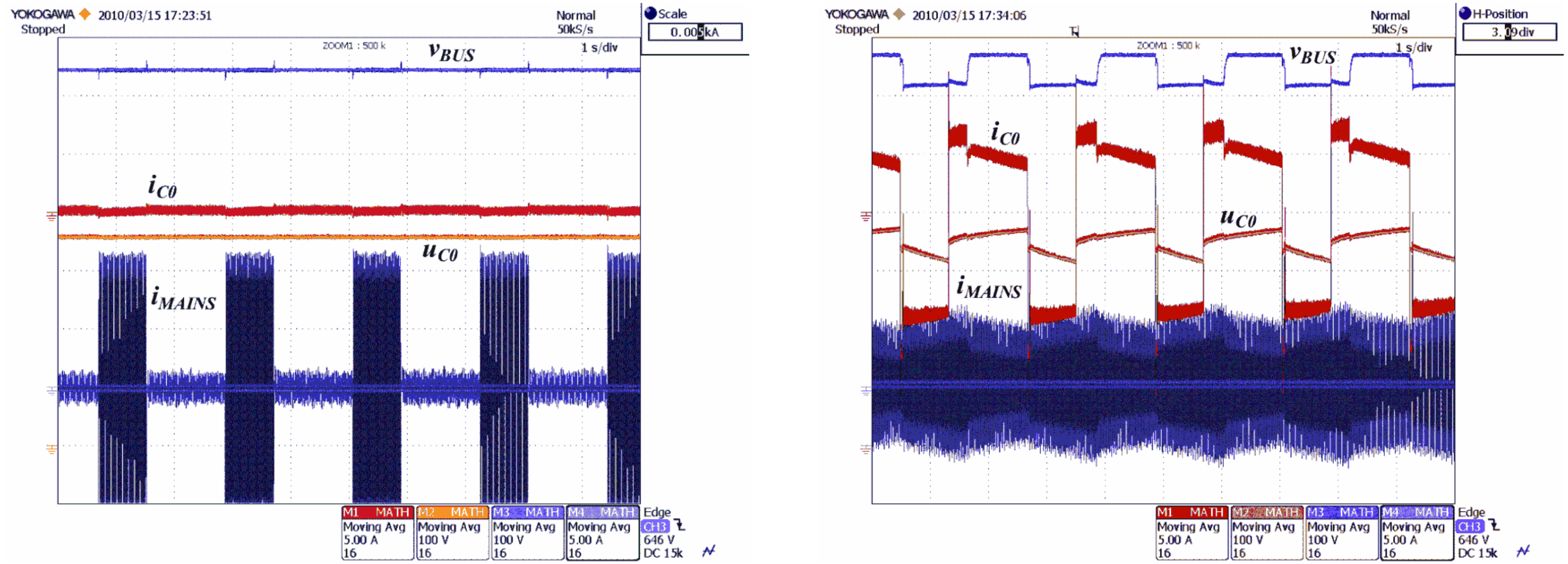
$$G_{C0}(s) = \left.\frac{u_{C0}(s)}{i_{C0}(s)}\right|_{\substack{i_{REC}(s)=0\\ p_{LOAD}(s)=0\\ v_{REC}(s)=0}} = R_{C0}\frac{s+\omega_Z}{s+\omega_P}$$

$$G_{BUS(C0)} = \left.\frac{v_{BUS}(s)}{i_{C0}(s)}\right|_{\substack{i_{REC}(s)=0\\ p_{LOAD}(s)=0\\ v_{REC}(s)=0}} = -\frac{(1+sC_{BUS}R_{ESR})(U_{C0}+I_{C0}R_{C0})}{sC_{BUS}V_{BUS}}$$

$$G_P(s) = \left.\frac{v_{BUS}(s)}{p_{LOAD}(s)}\right|_{\substack{i_{C0}(s)=0\\ i_{REC}(s)=0\\ v_{REC}(s)=0}} = -\frac{(1+sC_{BUS}R_{ESR})}{sC_{BUS}V_{BUS}}$$



The Converter Control



Experimental waveforms of the dc bus voltage V_{BUS} [100V/div], the mains current i_{MAINS} [5A/div] the ultra-capacitor current i_{C0} [5A/div] and voltage u_{C0} [100V/div].

The load is cycling (10% to 100% to 10%) $V_{BUS(REF)}$=650V, V_{MAINS}=400V, C_{BUS}=820µF,P_{LOAD}=5500W. a) f_{BOOST}=50Hz and b) f_{BOOST}=1Hz [4]

Conclusion

- Energy Storage Devices are today important and will be much more important in near future
- An **I**nterface **P**ower **C**onverter (***IPC***) is a MUST as a link between ES and the System
  - Small, Efficient and Cost Effective
    - New Devices (SiC and GaN) can be used but nor strictly required
    - New (OLD) Topologies are MUST
      - PPRC, Multi-Level, Multi-Cell, ISOP
      - CSC
      - Combinations of all above

Thank you very much for your attention!

petar.grbovic@uibk.ac.at